

# T14S/X13 Logic Schematics

Jazz2/Sideswipe2  
VER 1.0  
Aug/8/2019

BASE LOGIC 1 : Lightsaber-3 Pass-1 VER 0.25 Jul/10/2017  
BASE LOGIC 2 : Finn-1 SIT VER 2.01 Jun/28/2017

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2.BLOCK DIAGRAM

3.CPU (1/16): DDI/TYPE-C

4.CPU (2/16): DDR (1/2)

5.CPU (3/16): DDR (2/2)

6.CPU (4/16): MISC/JTAG

7.CPU (5/16): ESPI/SPI/SMBUS/C-LINK

8.CPU (6/16): LPSS/ISH

9.CPU (7/16): AUDIO/SDXC

10.CPU (8/16): PCIE/USB/SATA

11.CPU (9/16): CSI-2/EMMC/CNVI

12.CPU (10/16): CLOCK SIGNALS

13.CPU (11/16): SYSTEM PM

14.CPU (12/16): CPU POWER (1/2)

15.CPU (13/16): CPU POWER (2/2)

16.CPU (14/16): PCH POWER

17.CPU (15/16): GND

18.CPU (16/16): CFG/RESERVED

19.XDP CONNECTOR

20.RTC BATTERY

21.SPI FLASH

22.BLANK

23.BLANK

24.BLANK

25.BLANK

26.BLANK

27.BLANK

28.BLANK

29.BLANK

30.BLANK

31.BLANK

32.BLANK

33.DDR4 SUB CHANNEL-A

34.DDR4 SUB CHANNEL-B

35.DDR4 SUB CHANNEL-C
- 36.DDR4 SUB CHANNEL-D

37.BLANK

38.BLANK

39.BLANK

40.BLANK

41.BLANK

42.BLANK

43.BLANK

44.BLANK

45.BLANK

46.BLANK

47.BLANK

48.BLANK

49.BLANK

50.BLANK

51.LCD INTERFACE

52.LID/CAMERA/MIC/TOUCH INTERFACE

53.BLANK

54.HDMI CONNECTOR

55.ALPIKE RIDGE (1/2)

56.ALPIKE RIDGE (2/2)

57.BLANK

58..BLANK

59.USB PD CONTROLLER

60.BLANK

61.Type-C Switch

62.DOCKING CONNECTOR

63.THUNDERBOLT CONNECTOR

64.M.2 SOCKET 3 MODULE I/F

65.BLANK

66.M.2 TYPE 2230

67.M.2 SOCKET 2 MODULE I/F

68.DDI DEMUX/HDMI LEVEL SHIFTE

69.USB TYPE-A CONNECTOR

70.USB TYPE-A CONN

- 71.BLANK

72.Smart card reader/FRP/NEC LED

73.GBE JACKSONVILLE

74.BLANK

75.BLANK

76.MEDIA CARD CONTROLLER

77.MEDIA CARD INTERFACE

78.AUDIO ALC3287

79.AUDIO CONNECTOR

80.AUDIO JACK SENSE

81.AUDIO EXT MIC I/F

82.AUDIO SPEAKER

83.AUDIO BEEP

84.AUDIO Debug port

85.MEC1663(1/3)

86.MEC1663(2/3)

87.MEC1663(3/3)

88.KEYBOARD/TRACK POINT

89.TOUCH PAD/NFC

90.FAN CONNECTOR

91.APS G-SENSOR

92.BLANK

93.SMBUS SWITCH

94.THINK ENGINE-3 (1/2)

95..THINK ENGINE-3 (2/2)

96.BLANK

97.BLANK

98.DISCRETE TPM 2.0
- 99.SCREW HOLES

100.DC-IN

101.BATTERY INPUT

102.BATTERY CHARGER(BQ25700A)

103.DC/DC VCC5M (NB690)

104.DC/DC VCC5M\_PD (NB693)

105.DC/DC VCC3M (TPS51393)

106.BLANK

107.DC/DC VCC1R8\_SUS (BU90104)

108.DC/DC IMVP8 (MP2949AGQKT)

109.DC/DC VCCPCUCORE (MP86901C)

110.DC/DC VCCGFXCORE\_I (MP86901)

111.DC/DC VCCSA (MP86901A)

112.DC/DC VCC1R2A(NB687)

113.BLANK

114.DC/DC VCC1R05\_SUS(NB693)

115.BLANK

116.LOAD SW VCCST & VCCSTG

117.LOAD SW LAN

118.LOAD SW B

119.LOAD SW WLAN

120.LOAD SW PCH SUS

# JAZZ2/SIDESWIPE2 Block Diagram

Project Code: JAZZ2/Sideswipe2 2019 Jun ' 26

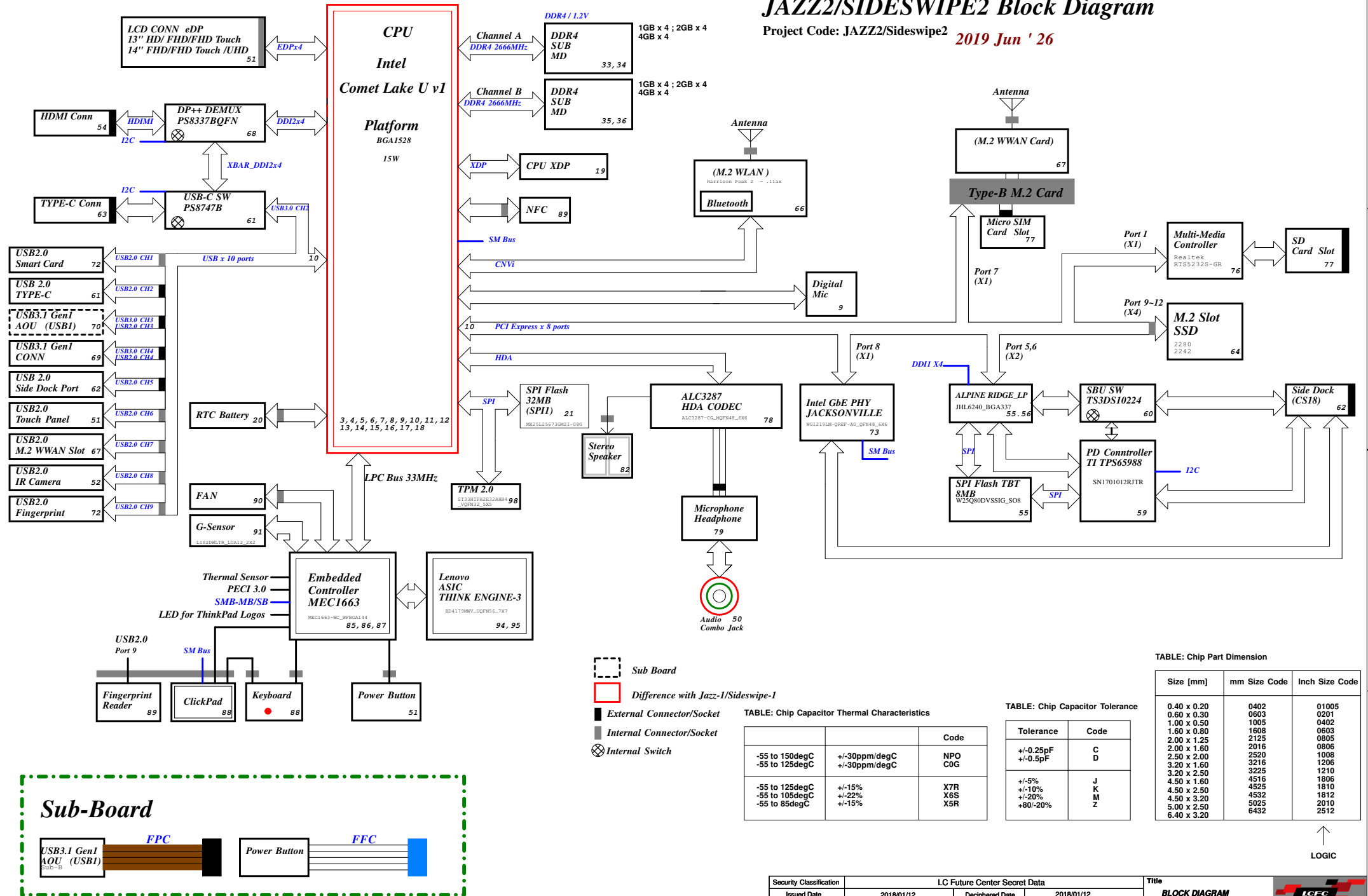
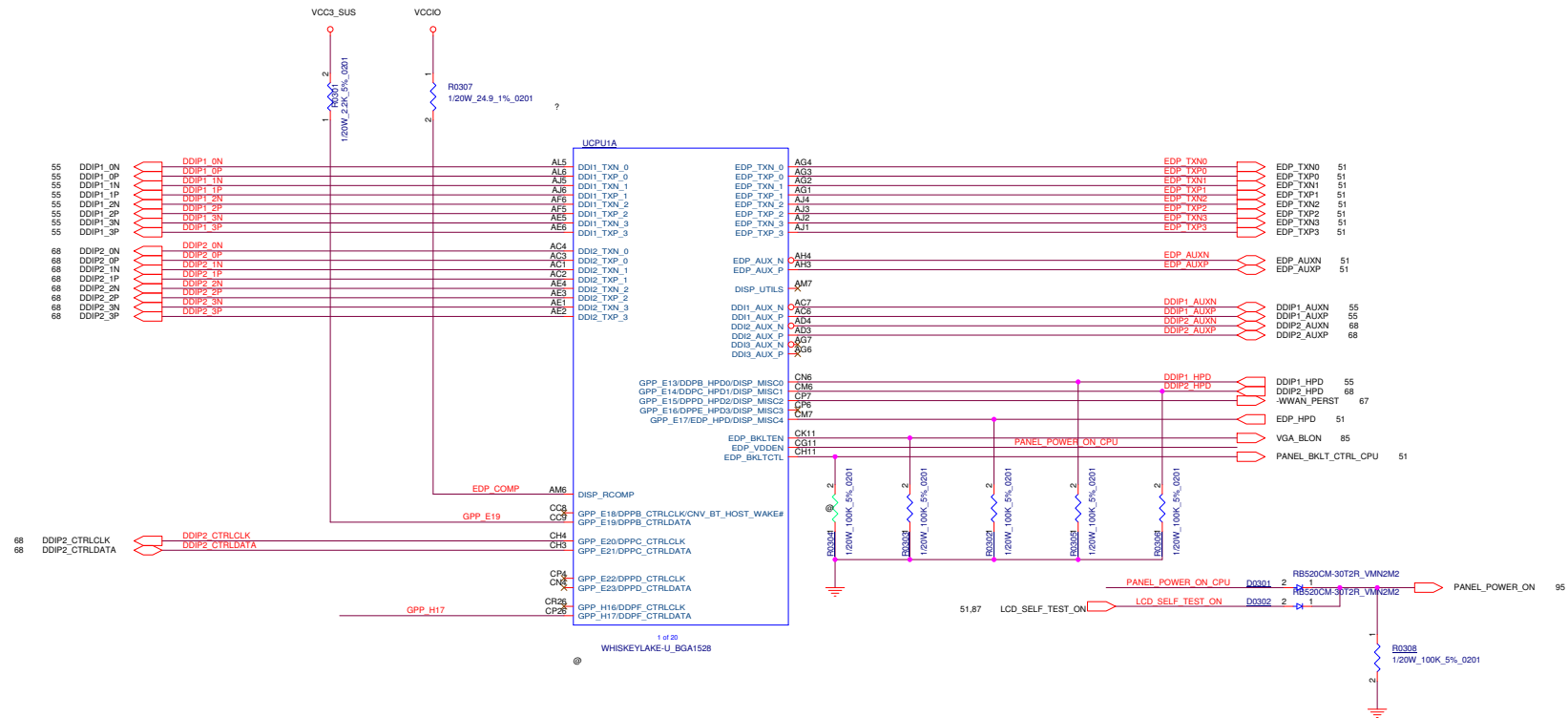
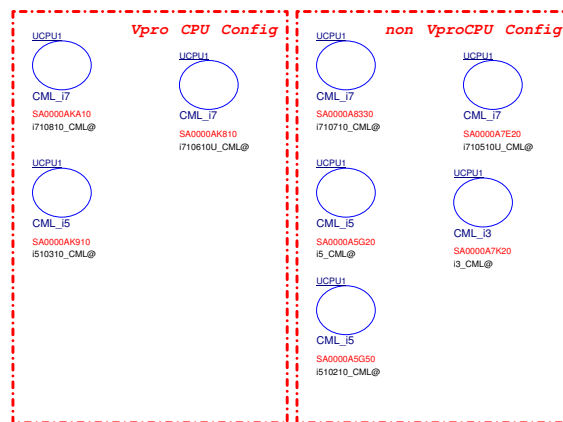
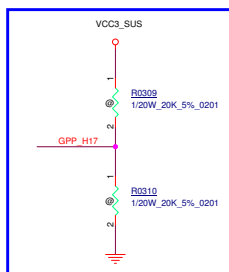
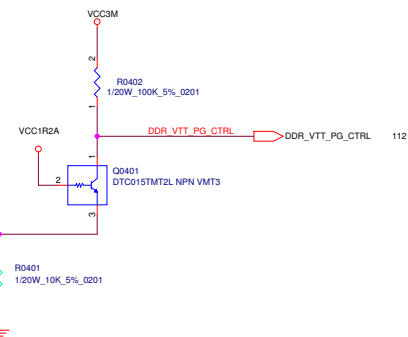
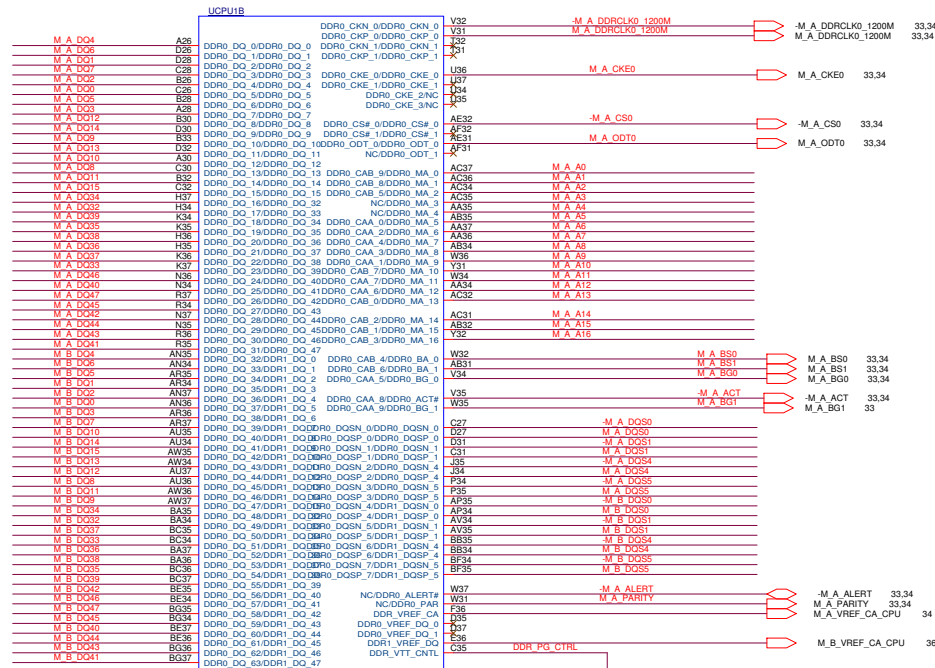




TABLE : Functional Strap

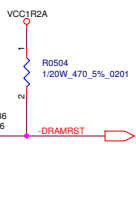
GPP_E19/DDP1_CTRLDATA/TBT_LSX0_RXD (DDP1 I2C / TBT LSX #0 PINS VCCIO CONFIGURATION)	
GPP_E21/DDP2_CTRLDATA/TBT_LSX1_RXD (DDP2 I2C / TBT LSX #1 PINS VCCIO CONFIGURATION)	
GPP_D10/DDP3_CTRLDATA/TBT_LSX2_RXD (DDP3 I2C / TBT LSX #2 PINS VCCIO CONFIGURATION)	
GPP_D12/DDP4_CTRLDATA/TBT_LSX3_RXD (DDP4 I2C / TBT LSX #3 PINS VCCIO CONFIGURATION)	
HIGH	3.3V
LOW	1.8V

1 of 30  
WHISKEYLAKE-U\_BGA1528

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				Date	Monday, February 10, 2020	Sheet	9 of 125



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				Date:	Monday, February 10, 2020, 15:00	Rev 0.1



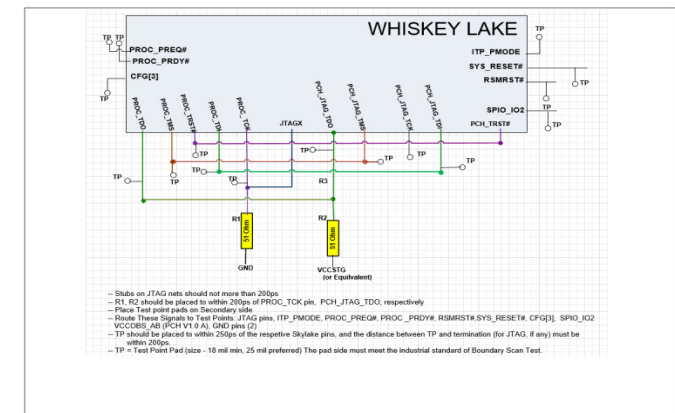
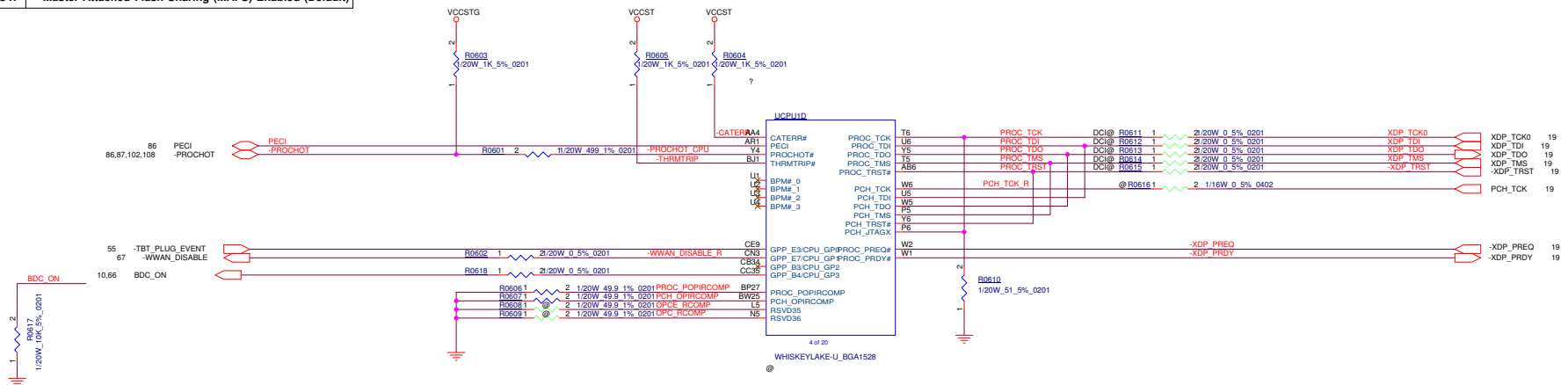
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				Rev	0.1

CPU SKU	U43e	U42
Pin A14	OPCE_RCOMP	Reserved
Pin B14	OPC_RCOMP	Reserved


ITP_PMODE (DFX Test Mode)	
HIGH	DFX Test Mode Disabled (Default)
LOW	DFX Test Mode Enabled

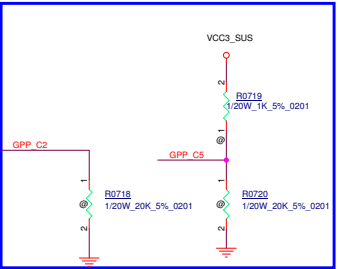
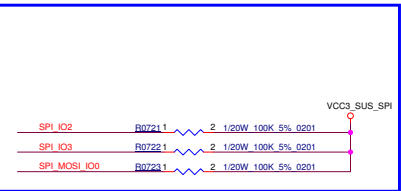
GPP_E6 (JTAG ODT Disable)	
HIGH	Enabled
LOW	Disabled

GPP_H2/CNV_BT_I2S_SDO (eSPI Flash Sharing Mode)	
HIGH	Slave Attached Flash Sharing (SAFS) Enabled
LOW	Master Attached Flash Sharing (MAFS) Enabled (Default)

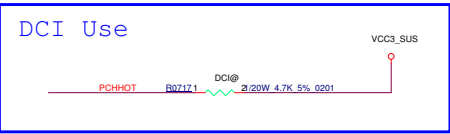
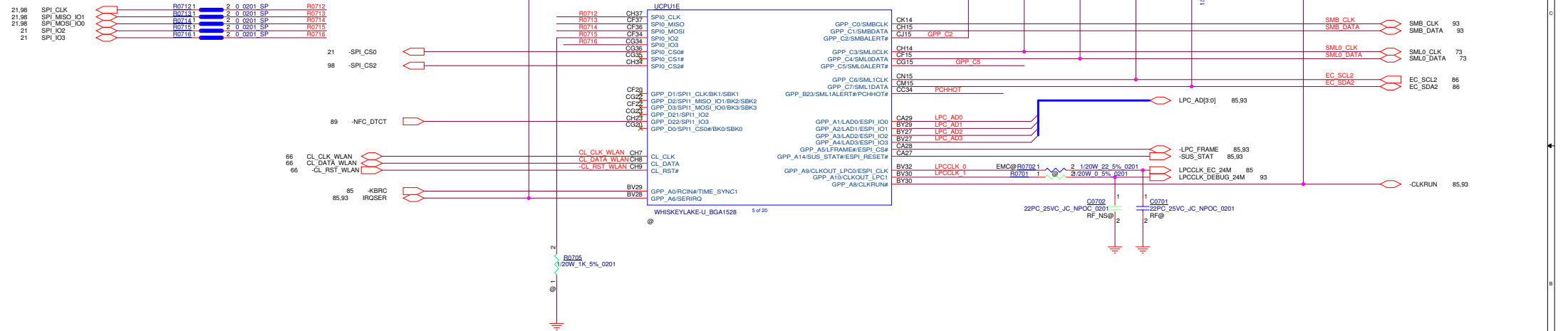


**Figure 13-6. Primary Debug PortConnector Less Routing Topology**

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Date:	Monday, February 19, 2020		15:00:00	124



R0712, R0713, R0714, R0715, R0716	SVT	PVT	SIT	SVT
Resistor	V	V	V	V
W-shield	V	V	V	V



<b>GPP_C2 / SMBALERT#</b>	TLS Confidentiality	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = <b>Disable</b> Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default) 1 = <b>Enable</b> Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS. <b>Notes:</b> 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
<b>SPI0_IO2</b>	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
<b>SPI0_IO3</b>	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
<b>SPI0_MOSI</b>	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

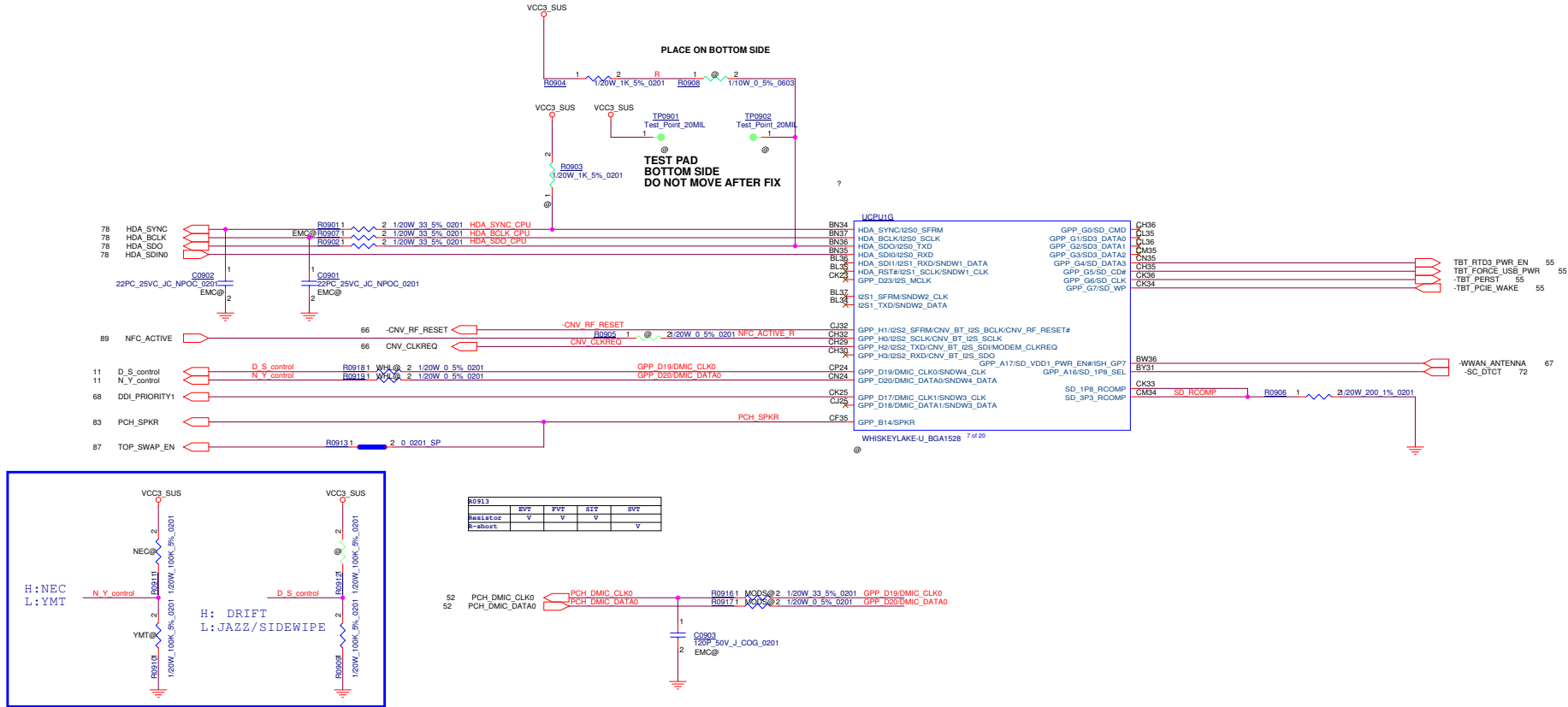
<b>GPP_B23 / SMBALERT# / PCHHOT#</b>	Intel® DCI-OOB	Rising edge of RSMRST#	This signal has an internal pull-down. 0 = Disable Intel® DCI-OOB (Default) 1 = Enable Intel® DCI-OOB <b>Notes:</b> 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. When used as PCHHOT# and strap low, a 150K pull-up is needed to ensure it does not override the internal pull-down strap sampling. This signal is in the primary well.
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		Date	Monday, February 10, 2020
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TABLE : Functional Strap	
HDA_SDO/I2S0_TXD	
Flash Descriptor Security Override	
HIGH	Disable Flash Descriptor Security (Override)
LOW	Enable Flash Descriptor Security (Default)





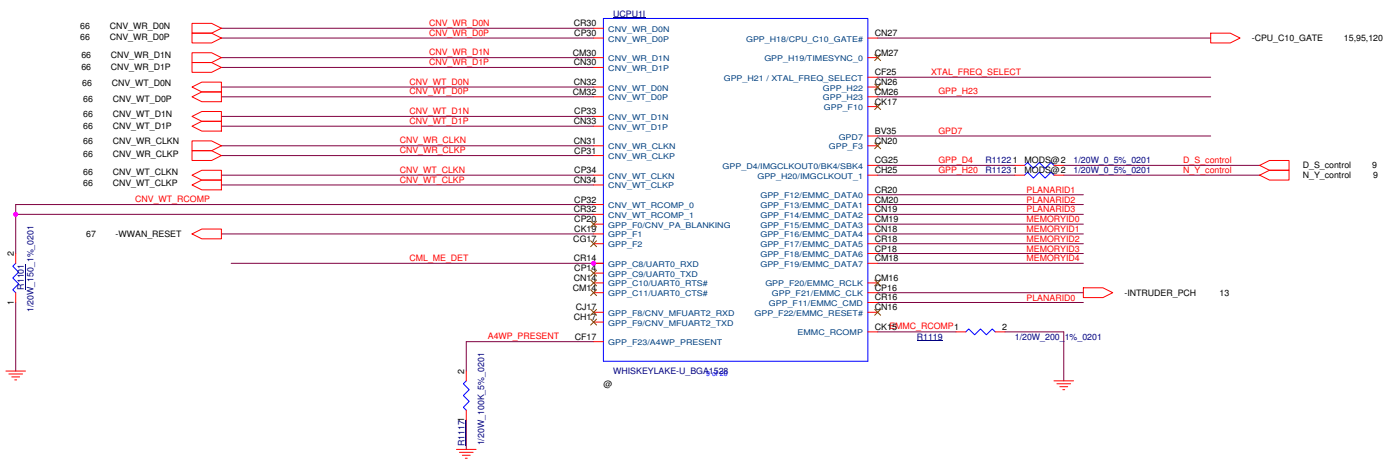
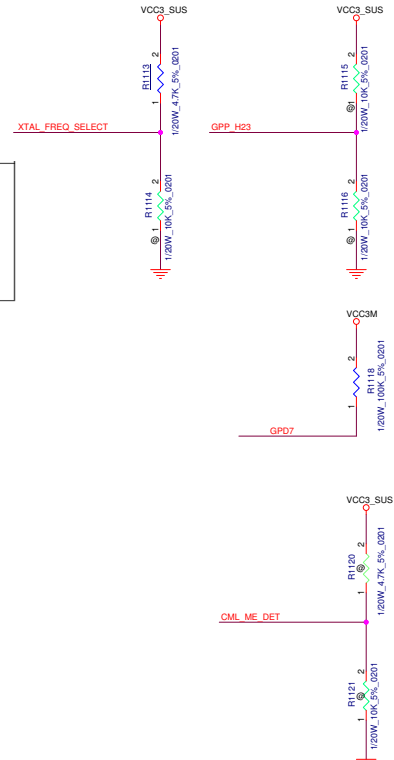
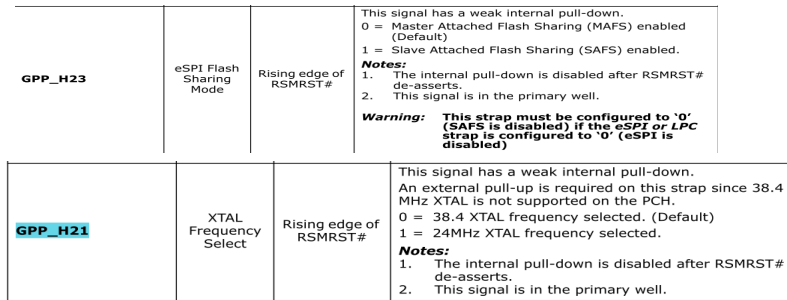


TABLE: MEMORYID							
MEMORYID[4:0]	Vendor	U3301, U3302, U3303, U3304, U3501, U3502, U3503, U3504					
		Part Number	Component	Qty	Channel-0	Channel-1	Total
00h (0000b)	Micron	SA00009R500	8Gbit SDP	4pcs	4GB	0GB	4GB
01h (0001b)		SA00009R500	8Gbit SDP	8pcs	4GB	4GB	8GB
02h (00010b)		SA0000ADK10	16Gbit DDP	8pcs	8GB	8GB	16GB
03h (00011b)	Samsung	SA0000AC820	8Gbit SDP	4pcs	4GB	0GB	4GB
04h (00100b)		SA0000AC820	8Gbit SDP	8pcs	4GB	4GB	8GB
05h (00101b)		SA0000AC000	16Gbit DDP	8pcs	8GB	8GB	16GB
06h (00110b)	SK hynix	SA0000AC720	8Gbit SDP	4pcs	4GB	0GB	4GB
07h (00111b)		SA0000AC720	8Gbit SDP	8pcs	4GB	4GB	8GB
08h (01000b)		SA0000AC500	16Gbit DDP	8pcs	8GB	8GB	16GB
09h (01001b)	Samsung	SA0000ACK00	32Gbit DDP	4pcs	16GB	0GB	16GB
10h (01010b)		SA0000ACK00	32Gbit DDP	8pcs	16GB	16GB	32GB
11h (01011b)		SA0000ADR00	32Gbit DDP	4pcs	16GB	0GB	16GB
12h (01100b)	Micron	SA0000ADR00	32Gbit DDP	8pcs	16GB	16GB	32GB

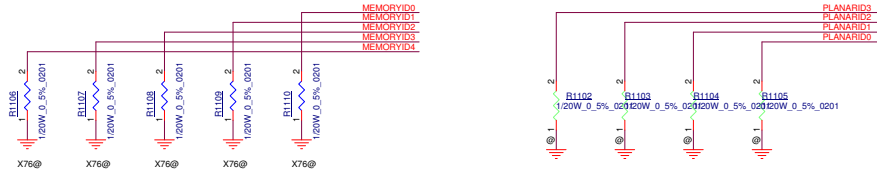
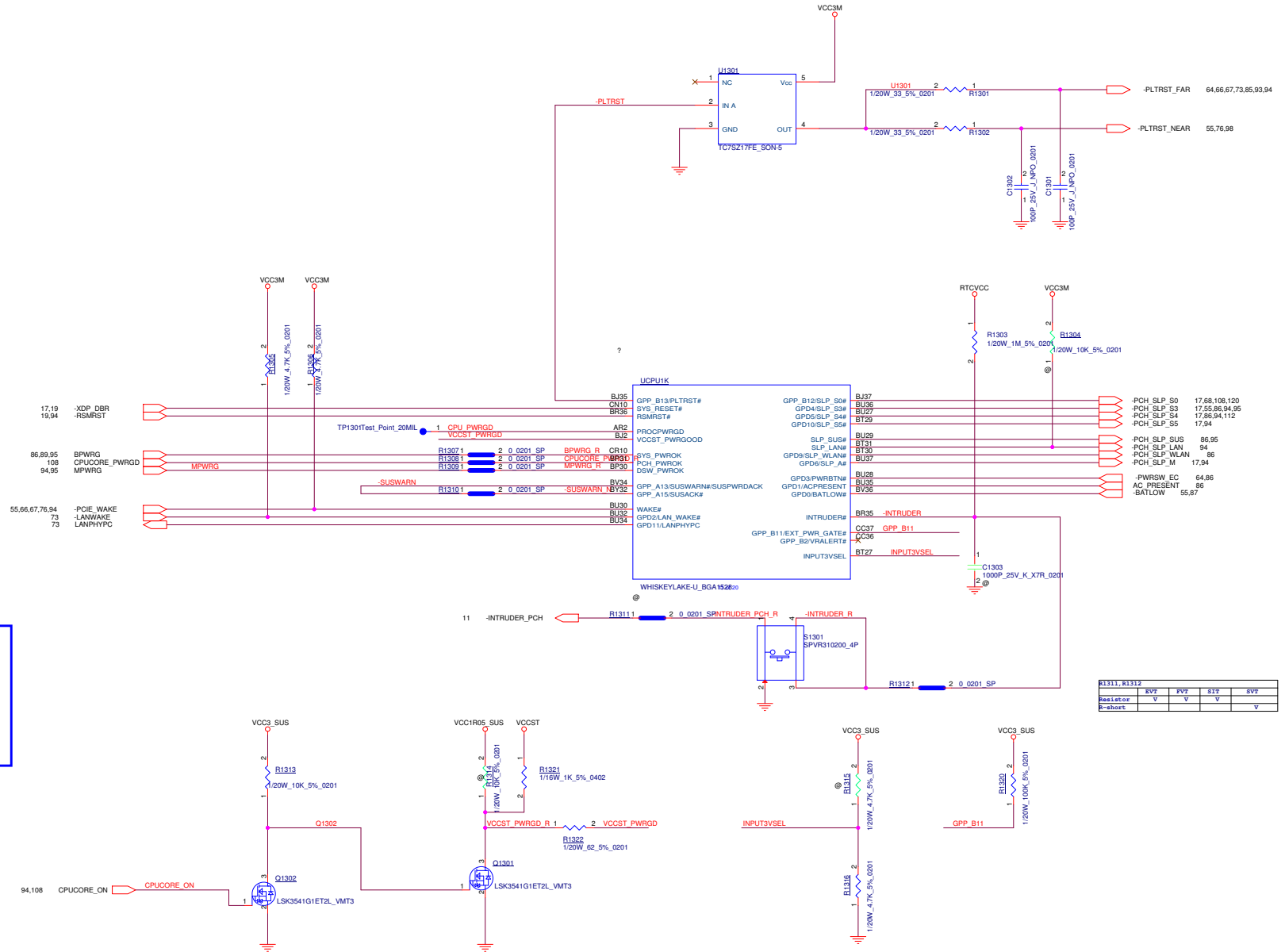
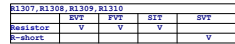


TABLE: PLANARID	
PLANARID[3:0]	PHASE
0h (0000b)	EVT
0h (0000b)	EVT2
1h (0001b)	FVT
2h (0010b)	SIT
Fh (1111b)	SVT



TABLE of U1301		
Vendor	P/N	LCFC P/N
ON	NL17SZ17XV5T2G	SA00005OU00
TI	SN74LVC1G17DRLR	SA00005MG00



R1311, R1312				
	EVT	FVT	SIT	SVT
Resistor	V	V	V	
R-short				V

**TABLE : Functional Strap**

INPUT3VSEL (VCCDSW_3P3)	
HIGH	3.0V
LOW	3.3V


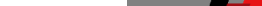
**TABLE : Functional Strap**

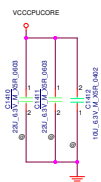
INTRUDER# (SPI Voltage Configuration)	
HIGH	SPI Voltage is 1.8V (Default)
LOW	SPI Voltage is 3.3V

TABLE : Functional Strap

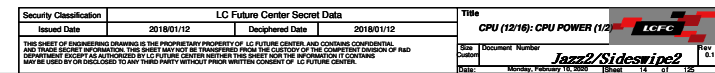
GPD7 (XTAL Input Mode)	
HIGH	XTAL Input is Single Ended
LOW	XTAL is Attached (Default)

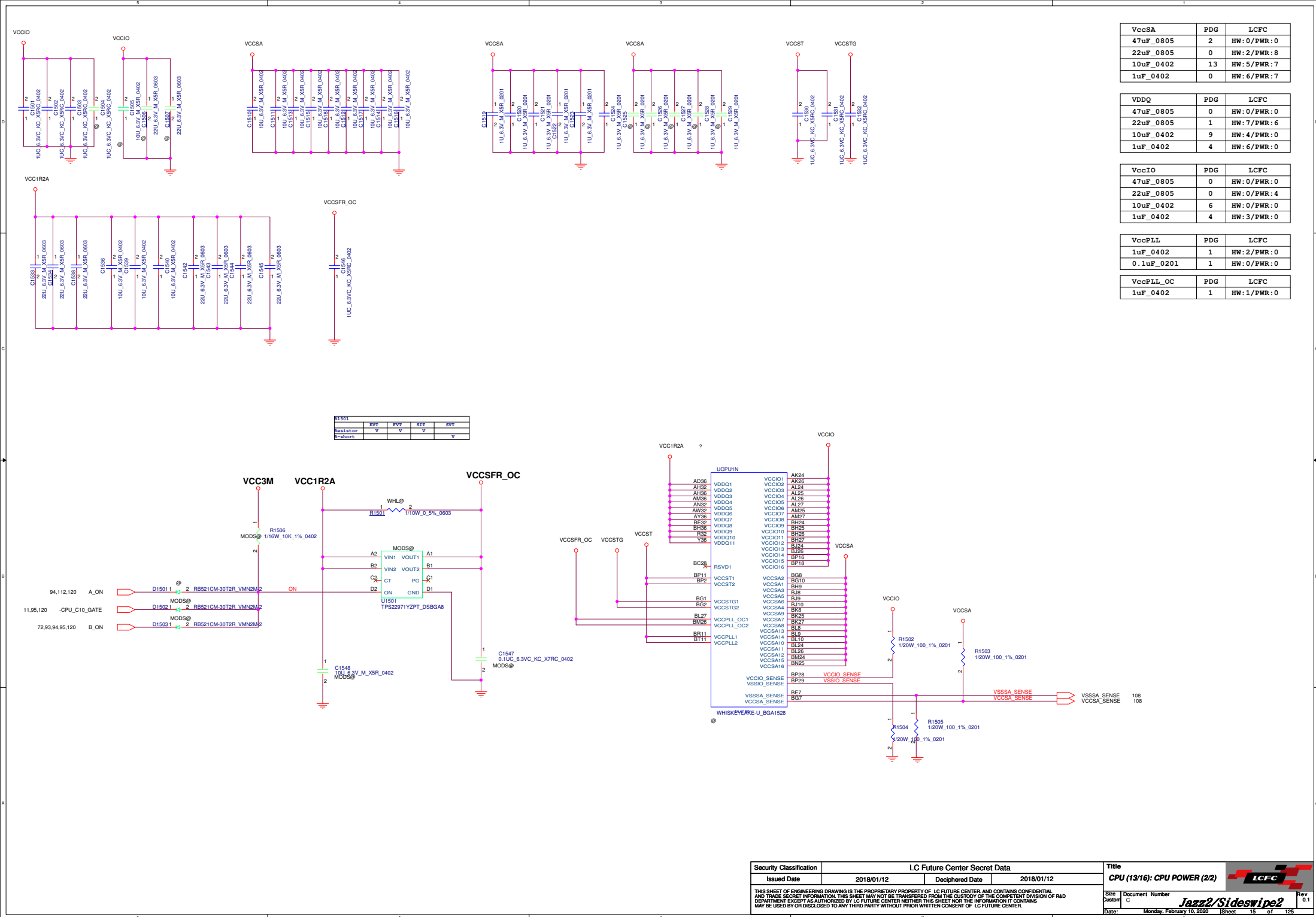
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				Date: Monday, February 10, 2020		13 of 125	



VccCORE	PDG	PDG
47uF_0805	18	HW:0/PWR:0
22uF_0603	9	HW:0/PWR:24
10uF_0402	22	HW:0/PWR:10
1uF_0402/0201	42	HW:0/PWR:10





VccSA	PDG	LCFC
47uF_0805	2	HW:0/PWR:0
22uF_0805	0	HW:2/PWR:8
10uF_0402	13	HW:5/PWR:7
1uF_0402	0	HW:6/PWR:7

VDDQ	PDG	LCFC
47uF_0805	0	HW:0/PWR:0
22uF_0805	1	HW:7/PWR:6
10uF_0402	9	HW:4/PWR:0
1uF_0402	4	HW:6/PWR:0

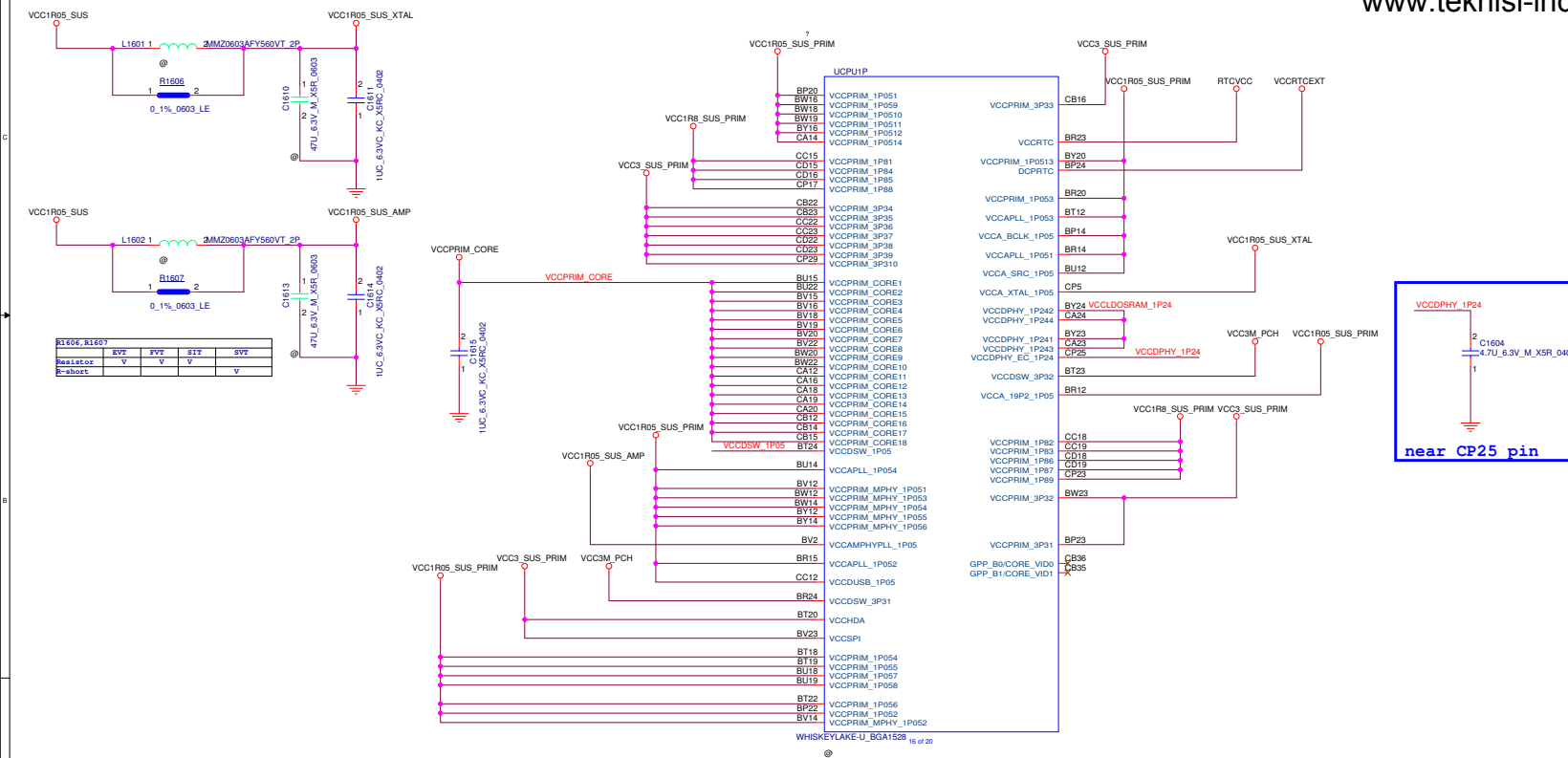
VccIO	PDG	LCFC
47uF_0805	0	HW:0/PWR:0
22uF_0805	0	HW:0/PWR:4
10uF_0402	6	HW:0/PWR:0
1uF_0402	4	HW:3/PWR:0

VccPLL	PDG	LCFC
1uF_0402	1	HW:2/PWR:0
0.1uF_0201	1	HW:0/PWR:0

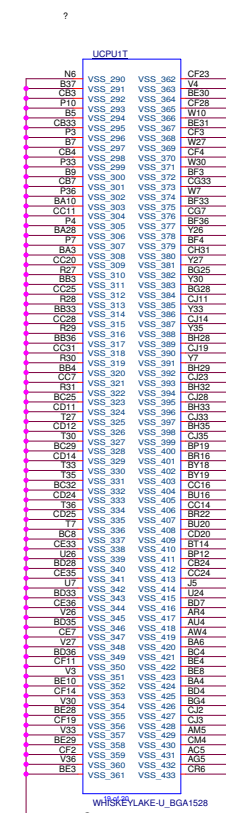
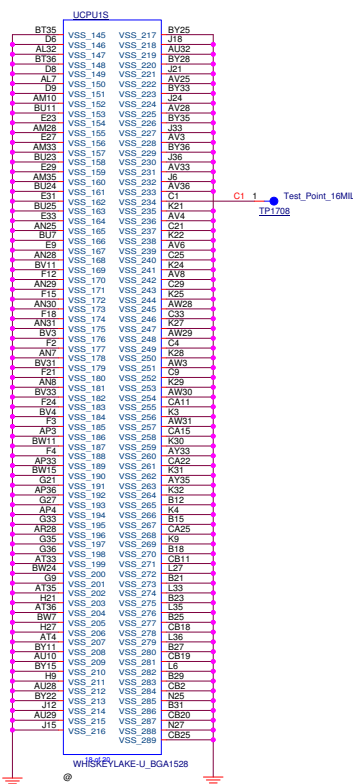
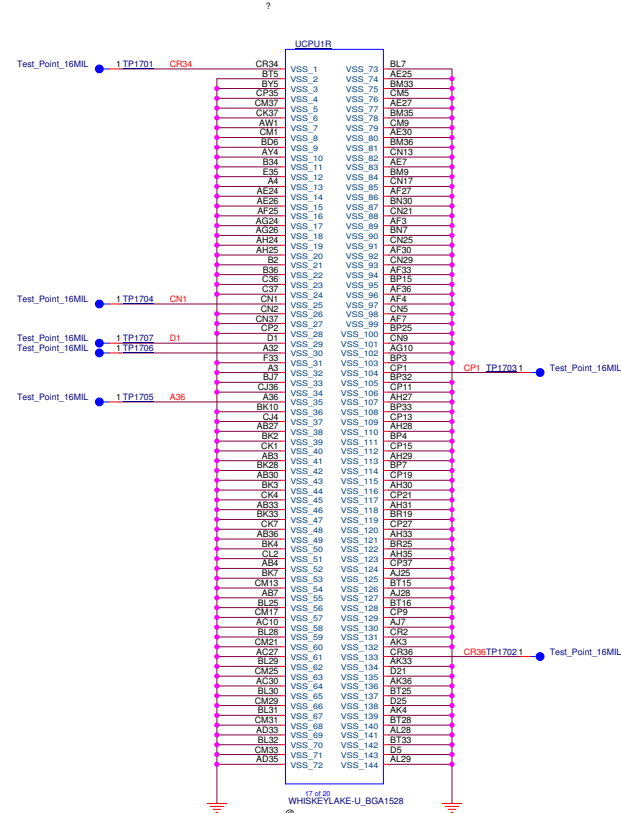
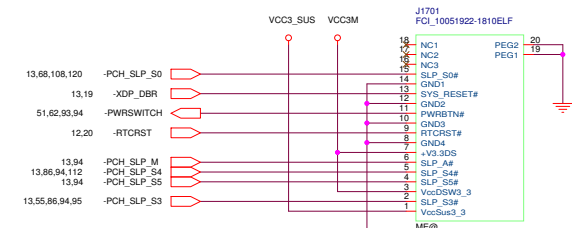
VccPLL_OC	PDG	LCFC
1uF_0402	1	HW:1/PWR:0


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Pinout diagram for J1701 (FOL1005/1922-1810ELF) showing connections for VCC3S, VCC3M, and VCC6. The diagram shows a 19-pin connector with pins 1 through 19. Pin 1 is connected to VCC3S. Pin 2 is connected to VCC3M. Pin 3 is connected to VCC6. Pin 4 is connected to VCC3S. Pin 5 is connected to VCC3M. Pin 6 is connected to VCC6. Pin 7 is connected to VCC3S. Pin 8 is connected to VCC3M. Pin 9 is connected to VCC6. Pin 10 is connected to VCC3S. Pin 11 is connected to VCC3M. Pin 12 is connected to VCC6. Pin 13 is connected to VCC3S. Pin 14 is connected to VCC3M. Pin 15 is connected to VCC6. Pin 16 is connected to VCC3S. Pin 17 is connected to VCC3M. Pin 18 is connected to VCC6. Pin 19 is connected to VCC3S.




<b>Security Classification</b>				<b>LC Future Center Secret Data</b>	<b>Title</b>		
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<b>Unit:mm</b>		<b>Auto:</b>		<b>Jazz2/Sideswipe2</b>		<b>0.1</b>	
		<b>Model: Eshelun</b>		<b>15-01-15</b>		<b>156</b>	

[illegible]PROC\_DETECT#  
/SKTOCC#

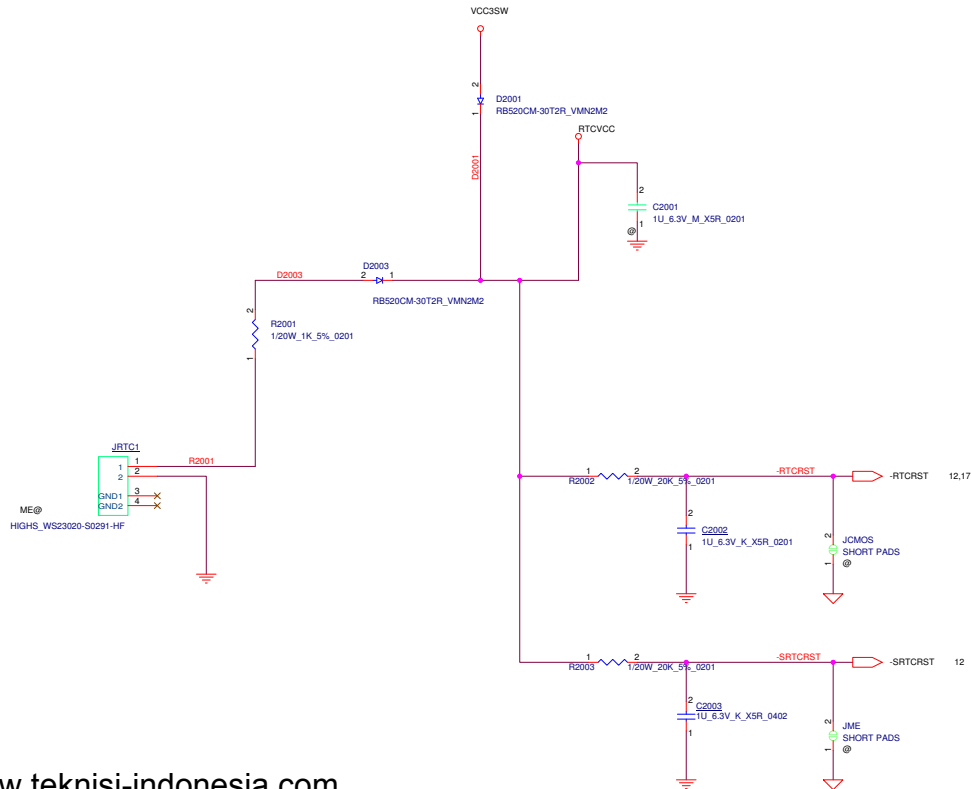
### Table 6-5. Reset and Miscellaneous Signals

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
CFG[19:0]	<p><b>Configuration Signals:</b> The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired.</p> <p>Intel recommends placing test points on the board for CFG pins.</p> <ul style="list-style-type: none"> <li>• <b>CFG[0]:</b> Stall reset sequence after PCU PLL lock until de-asserted: <ul style="list-style-type: none"> <li>— 1 = (Default) Normal Operation; No stall.</li> <li>— 0 = Stall.</li> </ul> </li> <li>• <b>CFG[1]:</b> Reserved configuration lane.</li> <li>• <b>CFG[2]:</b> PCI Express* Static x16 Lane Numbering Reversal. <ul style="list-style-type: none"> <li>— 1 = Normal operation</li> <li>— 0 = Lane numbers reversed.</li> </ul> </li> <li>• <b>CFG[3]:</b> Reserved configuration lane.</li> <li>• <b>CFG[4]:</b> eDP enable: <ul style="list-style-type: none"> <li>— 1 = Disabled.</li> <li>— 0 = Enabled.</li> </ul> </li> <li>• <b>CFG[6:5]:</b> PCI Express* Bifurcation <ul style="list-style-type: none"> <li>— 00 = 1 x8, 2 x4 PCI Express*</li> <li>— 01 = reserved</li> <li>— 10 = 2 x8 PCI Express*</li> <li>— 11 = 1 x16 PCI Express*</li> </ul> </li> <li>• <b>CFG[7]:</b> PEG Training: <ul style="list-style-type: none"> <li>— 1 = (default) PEG Train immediately following RESET# de assertion.</li> <li>— 0 = PEG Wait for BIOS for training.</li> </ul> </li> <li>• <b>CFG[19:8]:</b> Reserved configuration lanes.</li> </ul>	I	GTL	SE	U - Processor Lines CFG[2], CFG[6:5] and CFG[7] are not relevant for U - Processor Lines.



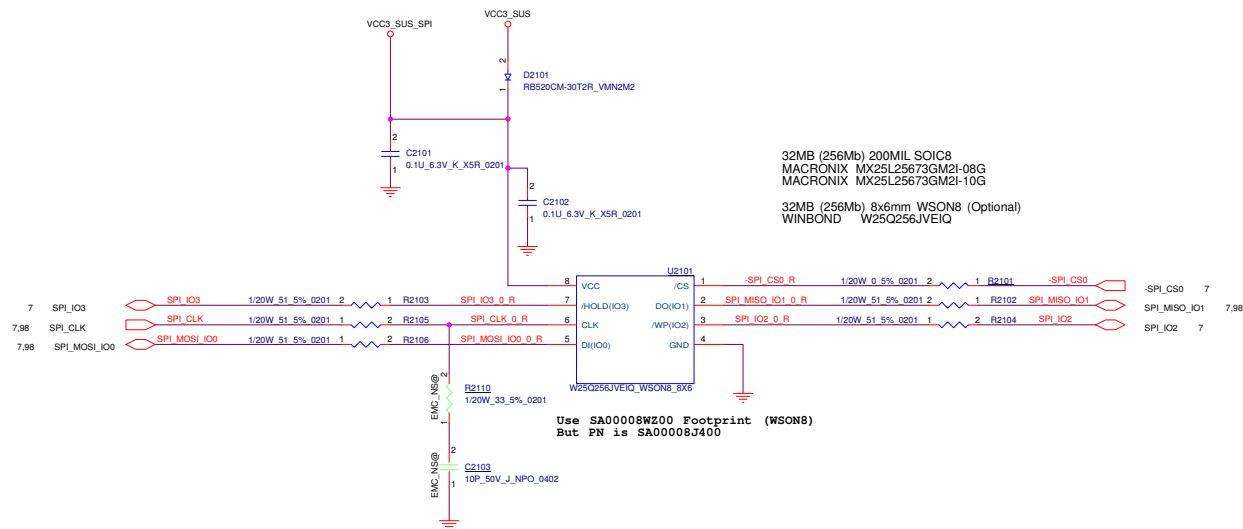
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32MB (256Mb) 200MIL SOIC8  
 MACRONIX MX25L25673GM2I-08G  
 MACRONIX MX25L25673GM2I-10G


32MB (256Mb) 8x6mm WSON8 (Optional)  
 WINBOND W25Q256JVEIQ

Use SA00008WZ00 Footprint (WSON8)  
 But PN is SA00008J400


TABLE of TPM (U2101)

Vendor	P/N	LCFC P/N
MXIC	FL 256M MX25L25673GM2I-08G	SA00008J400
WINBOND	FL 256M W25Q256JVEIQ WSON	SA00008WZ00
GigaDevice	256M GD25B256DY1GR WSON	SA00009R800


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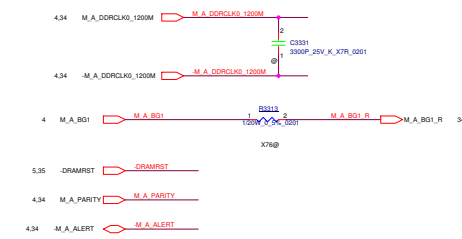
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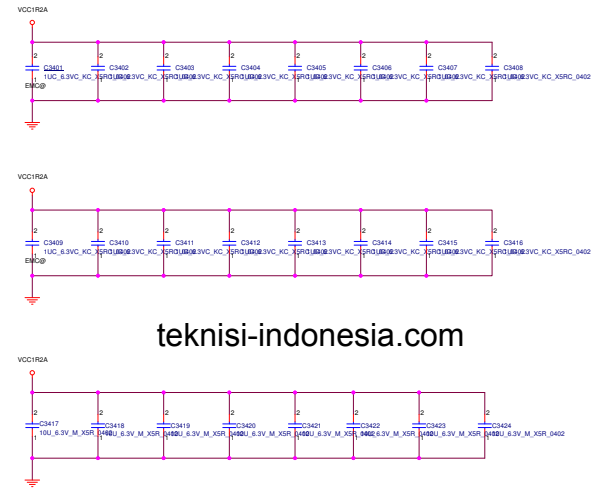
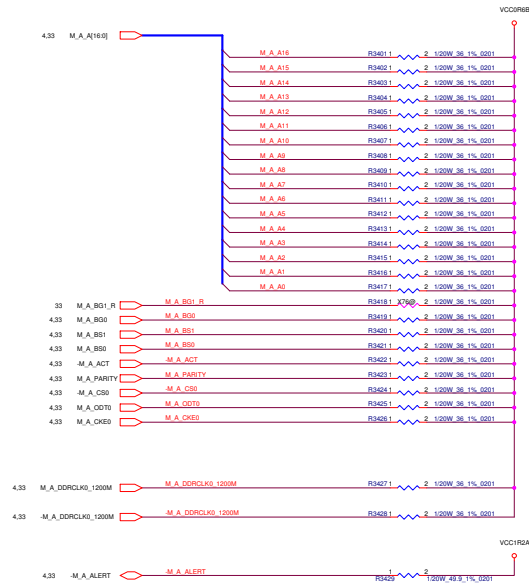
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R3304	ASM	NA
R3307	ASM	NA
R3310	ASM	NA
R3313	NA	ASM
R3418	NA	ASM
R3303	0.5%	243.1%
R3306	0.5%	243.1%
R3309	0.5%	243.1%
R3312	0.5%	243.1%

Supplier	Capacity	Supplier's P/N	LCFC P/N
Micron	8Gbit	MT40A512M16TB-062E-J	SA00009R500
	16Gbit	MT40A1G16KD-062E-E	SA0000A0DK10
Samsung	8Gbit	K4A8G16WCW-BCWE	SA0000AC820
	16Gbit	K4AAG165JCW-BCWE	SA00000AC00
SK hynix	8Gbit	HS58A86NCJR-XNC	SA0000AC720
	16Gbit	HS5ANAG6NMR-XNC	SA0000AC500
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Samsung	32Gbit	K4A8G165JCW-BCWA	SA00000AC00

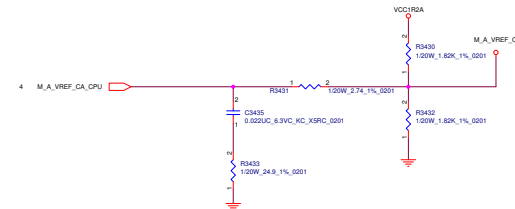
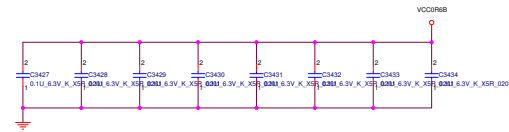
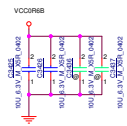
Supplier	Capacity	Supplier's P/N	Package Size	Die	Configuration	VSS_E9	BG1 / VSS	Single Ch	Dual Ch	
Micron	8Gbit	MT40A512M16TB-062E-J	7.5 x 13.5 mm	SDP	8Gb (512Mx16)	1 Rank x (512Mx16)	0.5%	VSS	4GB	8GB
	16Gbit	MT40A161G1K0D-062E-E	7.5 x 13.5 mm	DDP	16Gb (1Gx16)	1 Rank x (1Gx16)	243.1%	BG1	8GB	16GB
Samsung	8Gbit	K4A8G15WC-BCWE	7.5 x 13.3 mm	SDP	8Gb (512Mx16)	1 Rank x (512Mx16)	0.5%	VSS	4GB	8GB
	16Gbit	K4AAG15WA-BCWE	7.5 x 13.3 mm	DDP	16Gb (1Gx16)	1 Rank x (1Gx16)	243.1%	BG1	8GB	16GB
SK hynix	8Gbit	H5AN8G6NCJR-XNC	7.5 x 13.0 mm	SDP	8Gb (512Mx16)	1 Rank x (512Mx16)	0.5%	VSS	4GB	8GB
	16Gbit	H5ANAG6CMCR-XNC	7.5 x 13.0 mm	DDP	16Gb (1Gx16)	1 Rank x (1Gx16)	243.1%	BG1	8GB	16GB
Samsung	32Gbit	K4A8G165WA-BCWA	7.5 x 13.3 mm	DDP	16Gb (1Gx16)	1 Rank x (1Gx16)	243.1%	BG1	8GB	16GB
	32Gbit	MT40A2G16SKL-062E-B	7.5 x 13.5 mm	DDP	16Gb (1Gx16)	1 Rank x (1Gx16)	243.1%	BG1	8GB	16GB



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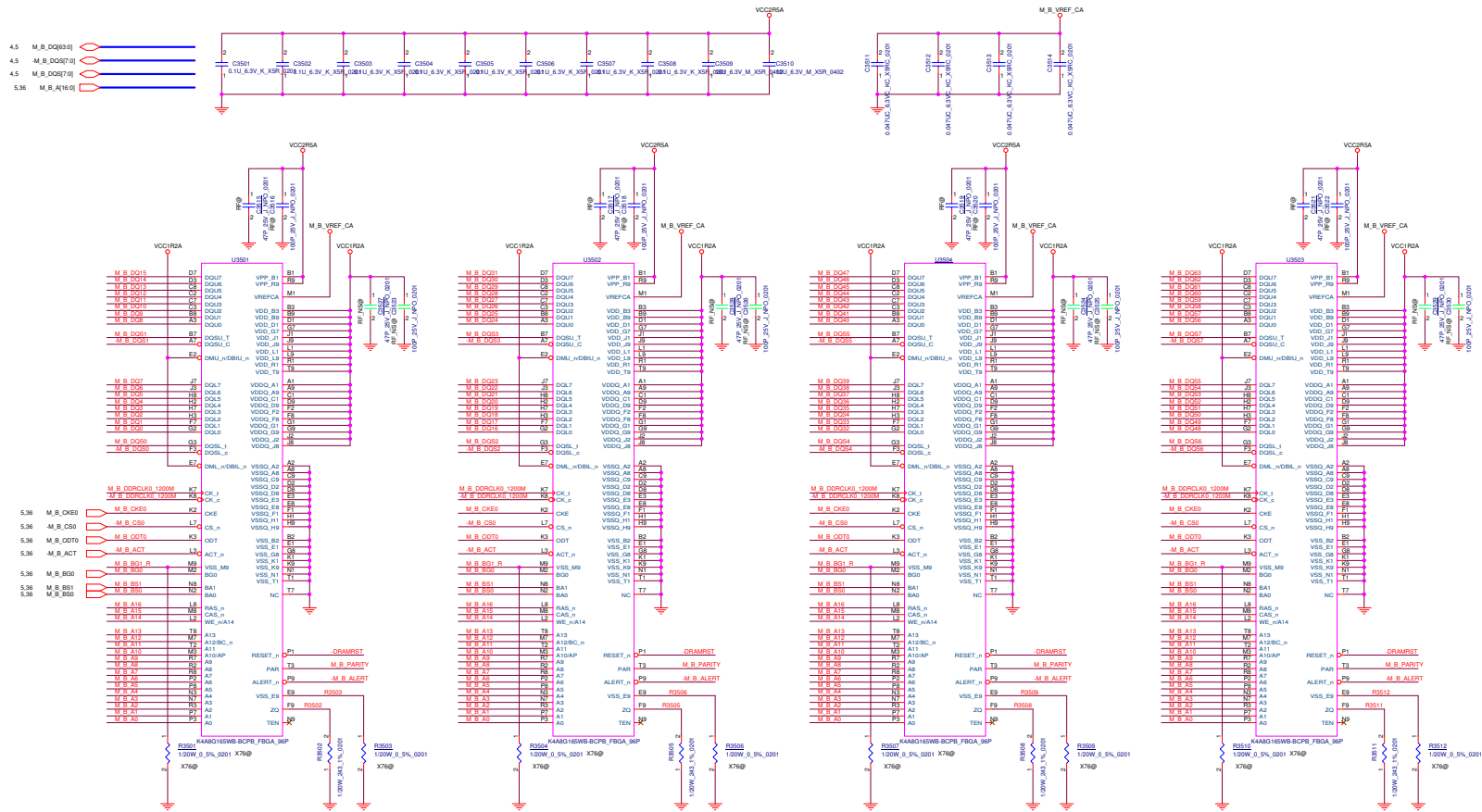


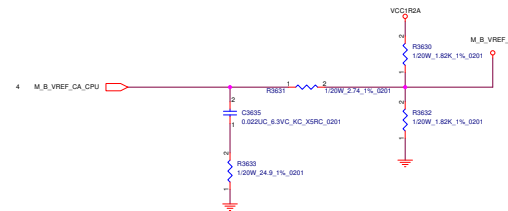
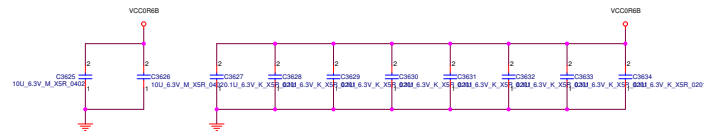
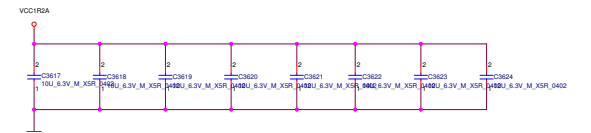
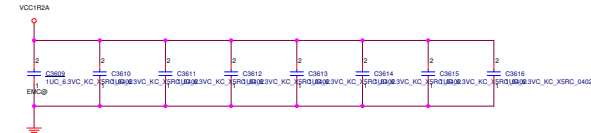
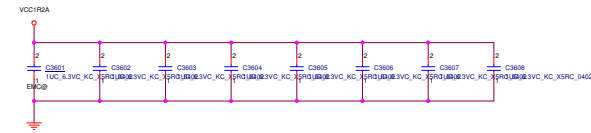
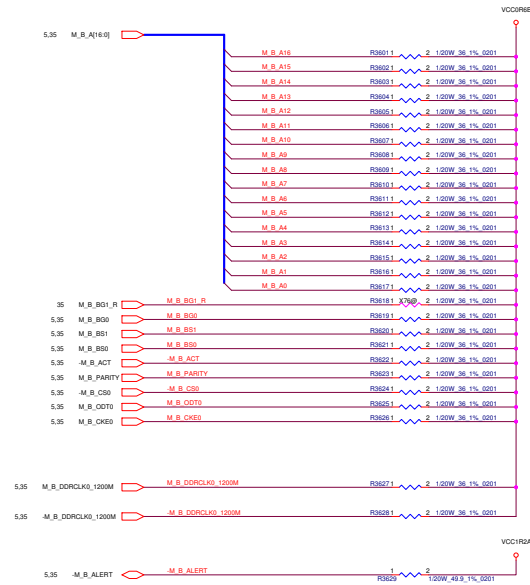
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R3504	ASM	NA
R3507	ASM	NA
R3510	ASM	NA
R3513	NA	ASM
R3518	NA	ASM
R3503	0.5%	243.1%
R3506	0.5%	243.1%
R3509	0.5%	243.1%
R3512	0.5%	243.1%

DRAM Configuration: X768


Supplier	Capacity	Supplier's P/N	LCFC P/N
Micron	8Gbit	MT40A512M16LY-075:E	SA00008P920
	16Gbit	MT40A1G16KNR-075:E	SA000090M00
Samsung	8Gbit	K4AAG165WC-BCTD	SA00008PE10
	16Gbit	K4AAG165WB-MCTD	SA00008WC10
SK hynix	8Gbit	HSAN8G6NCJR-VKC	SA000090T00
	16Gbit	TBD	

Supplier	Capacity	Supplier's P/N	Package Size	Die	Configuration	VSS_E9	BG1 / VSS	Single Ch	Dual Ch	
Micron	8Gbit	MT40A512M16LY-075-E	8.0 x 14.0 mm	SDP	8Gb (512Mx16)	1 Rank x (512Mx16)	0.5%	VSS	4GB	8GB
	16Gbit	MT40A1G16KNR-075-E	8.0 x 14.0 mm	DDP	16Gb (1Gx16)	1 Rank x (1Gx16)	243.1%	BG1	8GB	16GB
Samsung	8Gbit	K4AAG165WC-BCTD	7.5 x 13.3 mm	SDP	8Gb (512Mx16)	1 Rank x (512Mx16)	0.5%	VSS	4GB	8GB
	16Gbit	K4AAG165WB-MCTD	7.5 x 13.3 mm	DDP	16Gb (1Gx16)	1 Rank x (1Gx16)	243.1%	BG1	8GB	16GB
SK hynix	8Gbit	HSAN8G6NCJR-VKC	7.5 x 13.3 mm	SDP	8Gb (512Mx16)	1 Rank x (512Mx16)	0.5%	VSS	4GB	8GB
	16Gbit	TBD		DDP						




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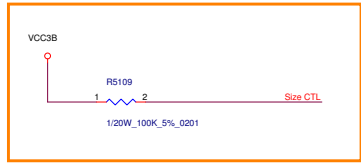
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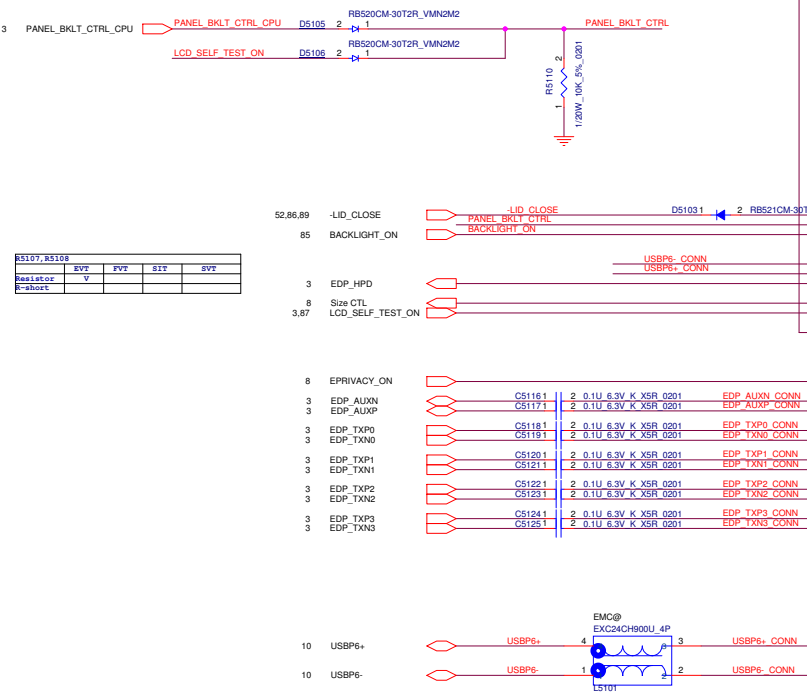
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LCD size control  
Low: 14" JAZZ  
High: 13" SIDESWIPE

R5107, R5108	RVS	PVS	SIZ	SVS
Resistor	V			
K-shoot				

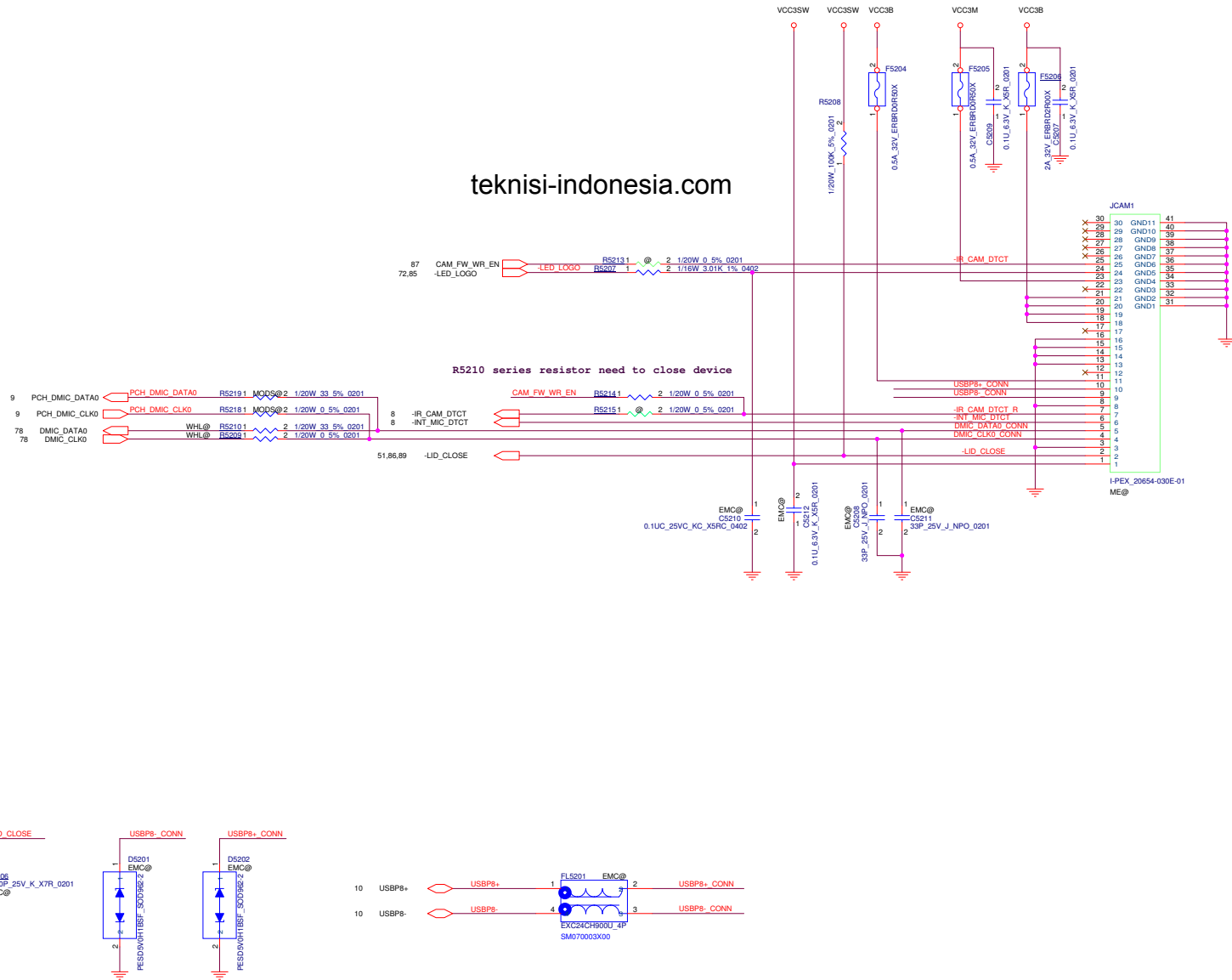


## LCD CONNECTOR

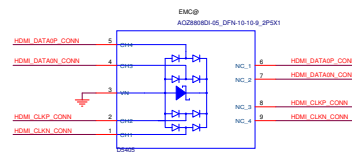
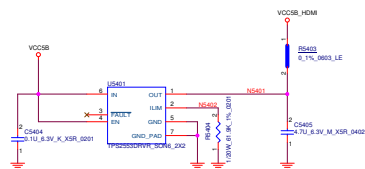


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	EVT	FVT	SIT	SVT
Realizator	V	V	V	
Substrat				

R5503		BV?	PV?	SV?	SV?
Resistor	V	V	V	V	V
Short					

12	PCIES_CLK_100M				
12	-PCIES_CLK_100M				
12	-CLKREQ_PCIES				
3	DDI01_0P				
3	DDI01_0N				
3	DDI01_1P				
3	DDI01_1N				
3	DDI01_2P				
3	DDI01_2N				
3	DDI01_3P				
3	DDI01_3N				
3	DDI01_AUXP				
3	DDI01_AUXN				
3	DDI01_HPD				

@TP5501Test\_Point\_20MIL 1

VCC3 TBT\_LC

62 TBT\_RX2P  
62 TBT\_RX2N  
62 TBT\_TX2P  
62 TBT\_TX2N  
62 TBT\_TX1P  
62 TBT\_TX1N  
62 TBT\_RX1P  
62 TBT\_RX1N  
60 TBT\_AUXP  
60 TBT\_AUXN  
60 TBT\_LSTX  
60 TBT\_LSRX  
50 TBT\_HPD

VCC3\_SUS

DPSRC_CTRLCLK	R5530	1	2/20W 100K 5% 0201
DPSRC_CTRLCLK	R5531	1	2/20W 100K 5% 0201
TBT_TMUI_CLK_OUT	R5534	1	2/20W 100K 5% 0201
TBT_FORCE_PWR	R5536	1	2/18W 10K 5% 0402
TBT_RT03_USB_PWR_EN	R5538	1	2/20W 10K 5% 0201
-BATLOW TBT	R5540	1	2/20W 10K 5% 0201
-PCH_SLP_S3_TBT	R5542	1	2/20W 10K 5% 0201
-TBT_EE_WP	R5544	1	2/20W 10K 5% 0201
TBT_RT03_CIO_PWR_EN	R5546	1	2/20W 10K 5% 0201

Vendor	P/N	LCFC P/N
TXC	8Y25000004	SJ10000H00J
KDS	1ZZHAE25000CCOF	SJ10000P300

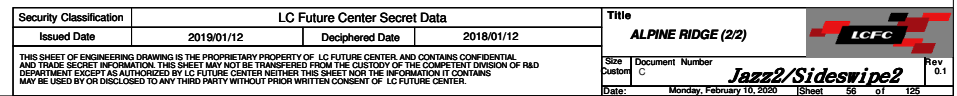
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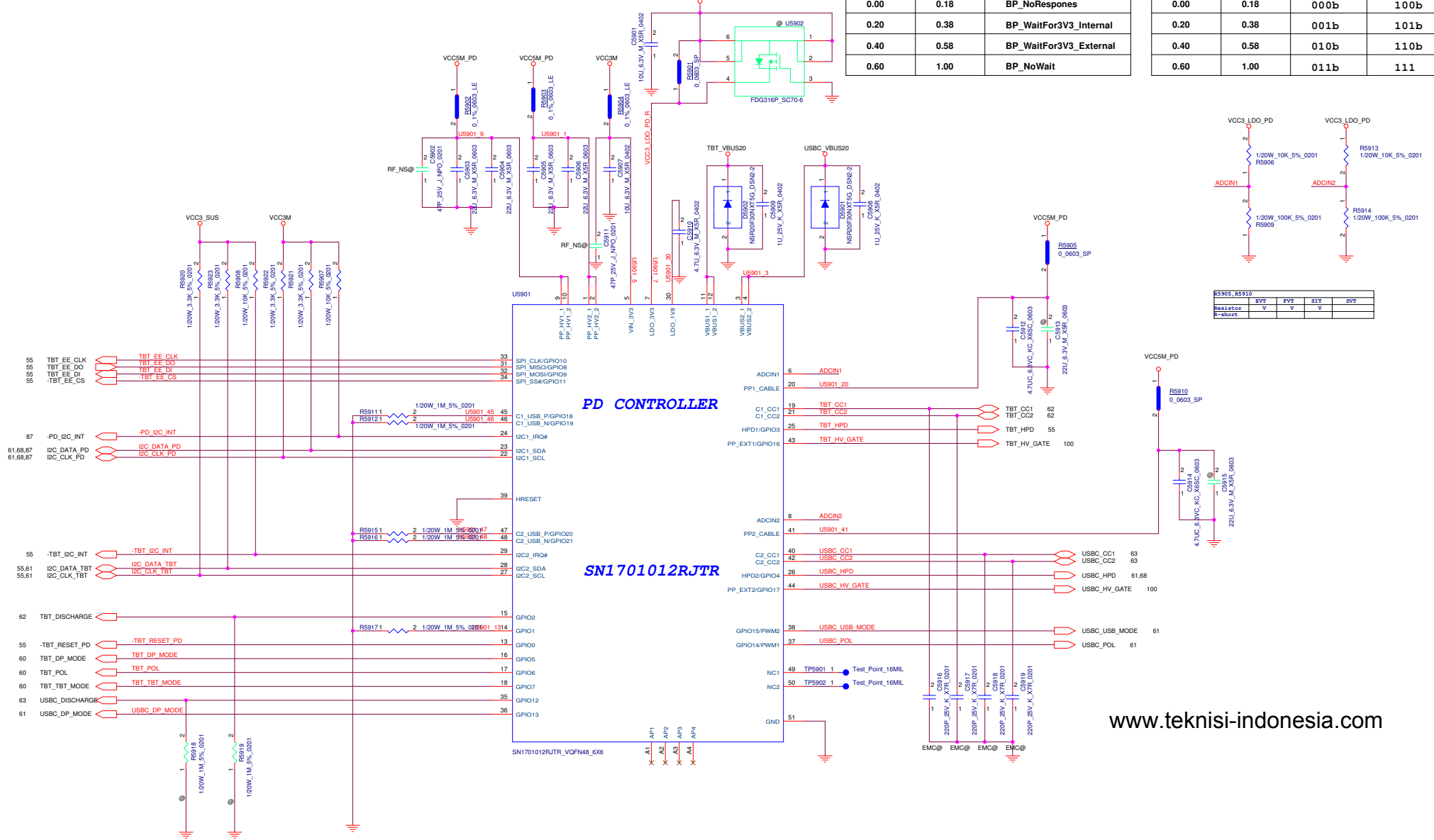
R5901, R5902, R5903, R5904				
Resistor	SVT	PVT	STV	SVT
0-short	V	V	V	V

TABLE BUSPOWER Configuration - ADCIN1

DIV = R2/ (R1+R2)		Configuration
DIV MIN	DIV MAX	
0.00	0.18	BP_NoResponses
0.20	0.38	BP_WaitFor3V3_Internal
0.40	0.58	BP_WaitFor3V3_External
0.60	1.00	BP_NoWait

TABLE BUSPOWER Configuration - ADCIN2

DIV = R2/ (R1+R2)		I2C Unique Address [3:1]	
DIV MIN	DIV MAX	I2C_ADDR_DECODE_C1	I2C_ADDR_DECODE_C2
0.00	0.18	000b	100b
0.20	0.38	001b	101b
0.40	0.58	010b	110b
0.60	1.00	011b	111b



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R6003, R6001, R6004				
RVF	RVF	SVF	SVF	SVF
Resistor	V	V	V	V
Short				

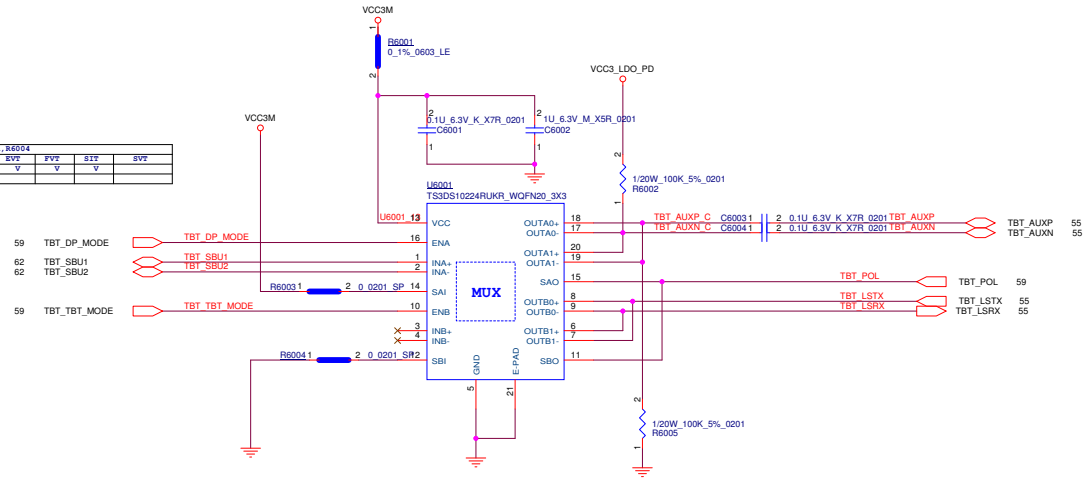
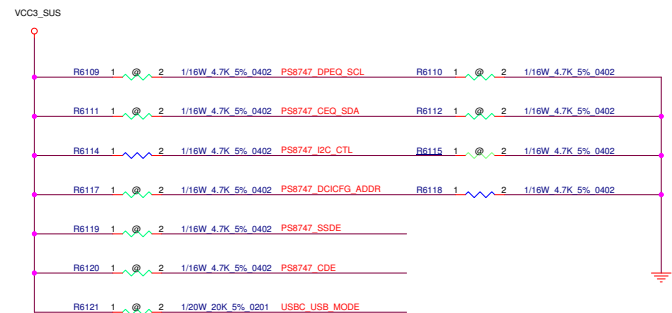
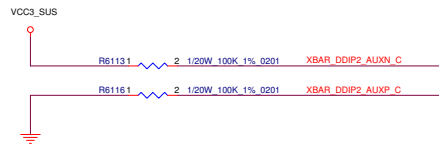
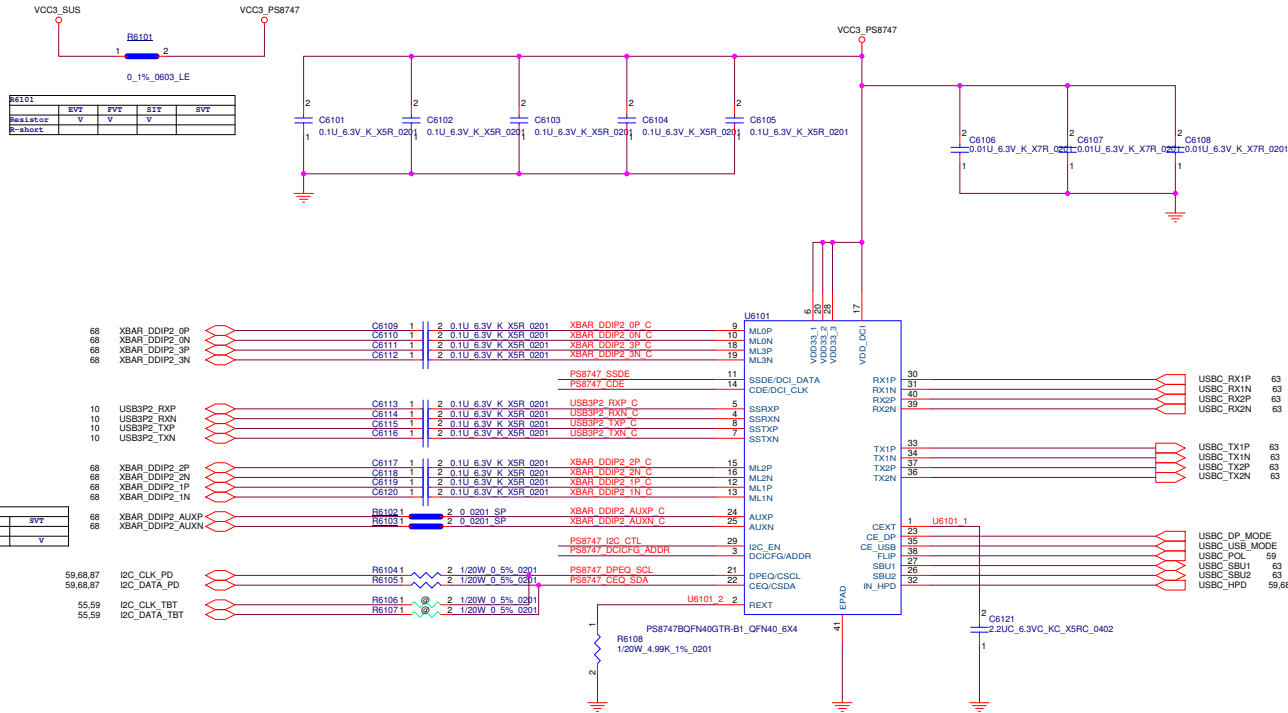
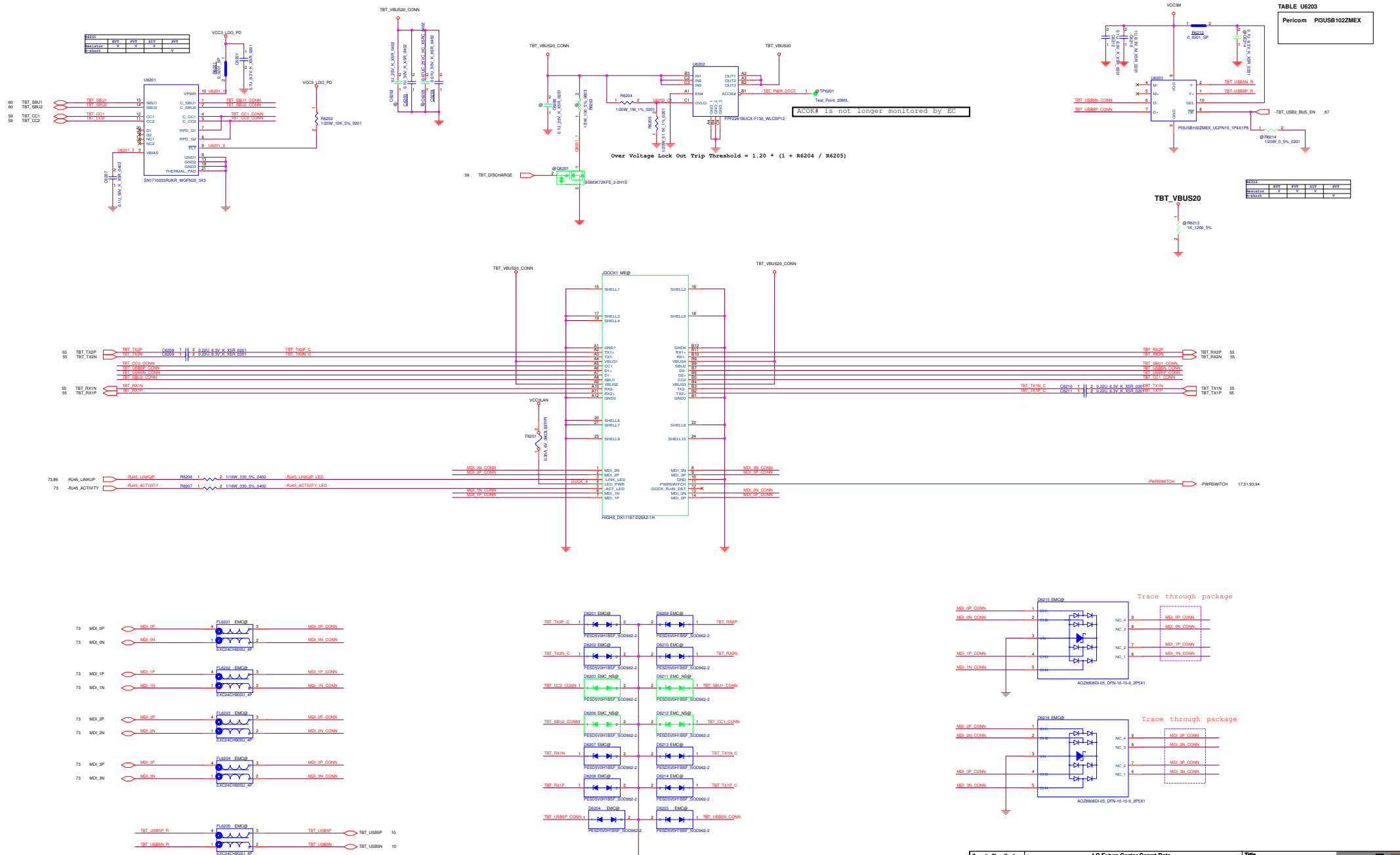


TABLE of U6001		
Vendor	P/N	LCFC P/N
T1	TS3DS10224RUKR	SA00008AS00
DIODES	PI3DBS3224ZNAEX	SA00008CC00





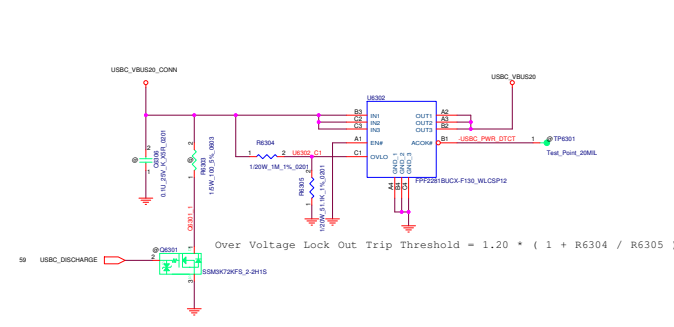
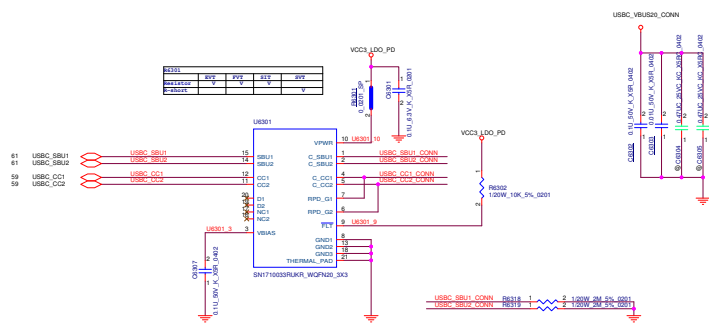
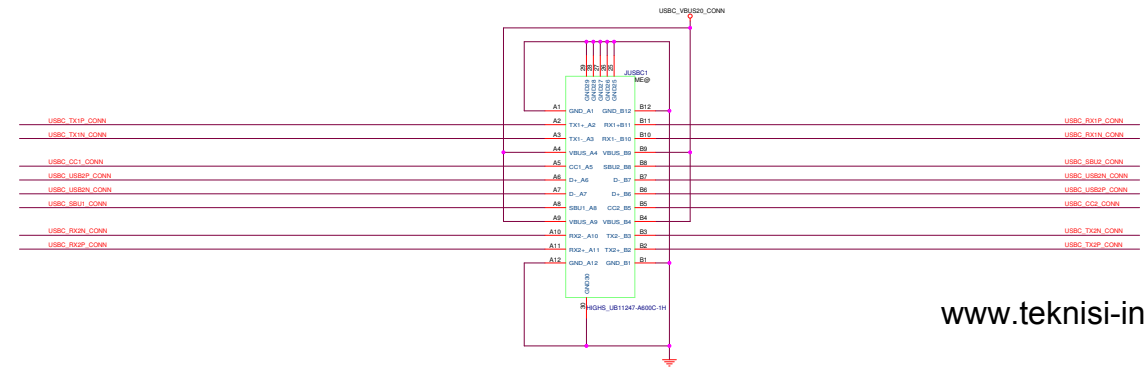
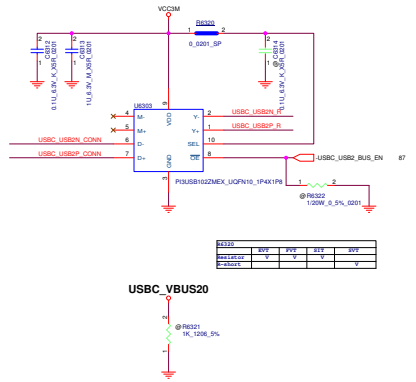
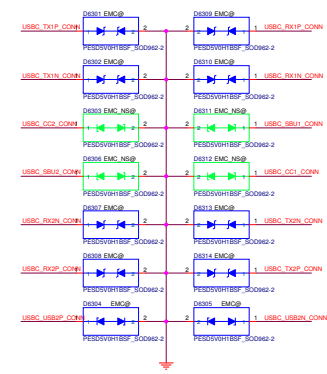
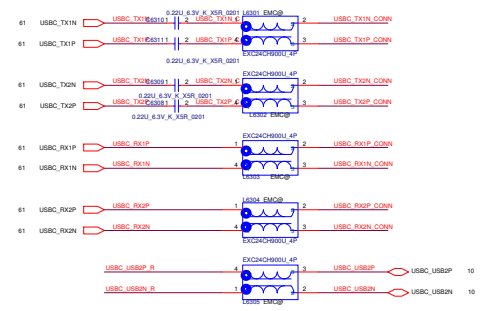


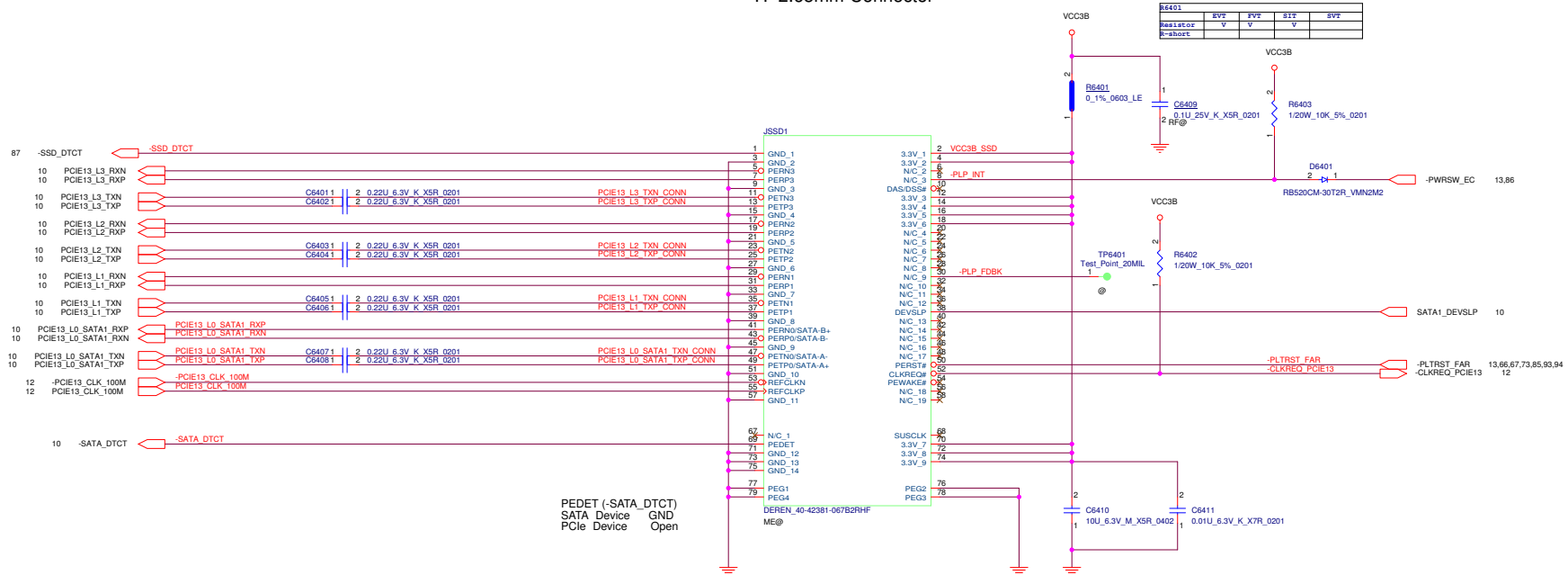
TABLE U6303  
Pericom PI3USB102ZMEX



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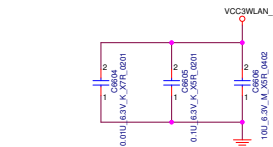
# M.2 Socket 3 (Key-M) for 2280 S3 SSD H=2.65mm Connector





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Platform	CNVio	PCH IP	REFCLK
Whiskey Lake	Gen1	Pulsar	38.4MHz Clock form JfP Module
Ice Lake	Gen2	Quasar	Generated inside SoC

C6601,C6602,C6603 close to M.2 pin 4 and pin5



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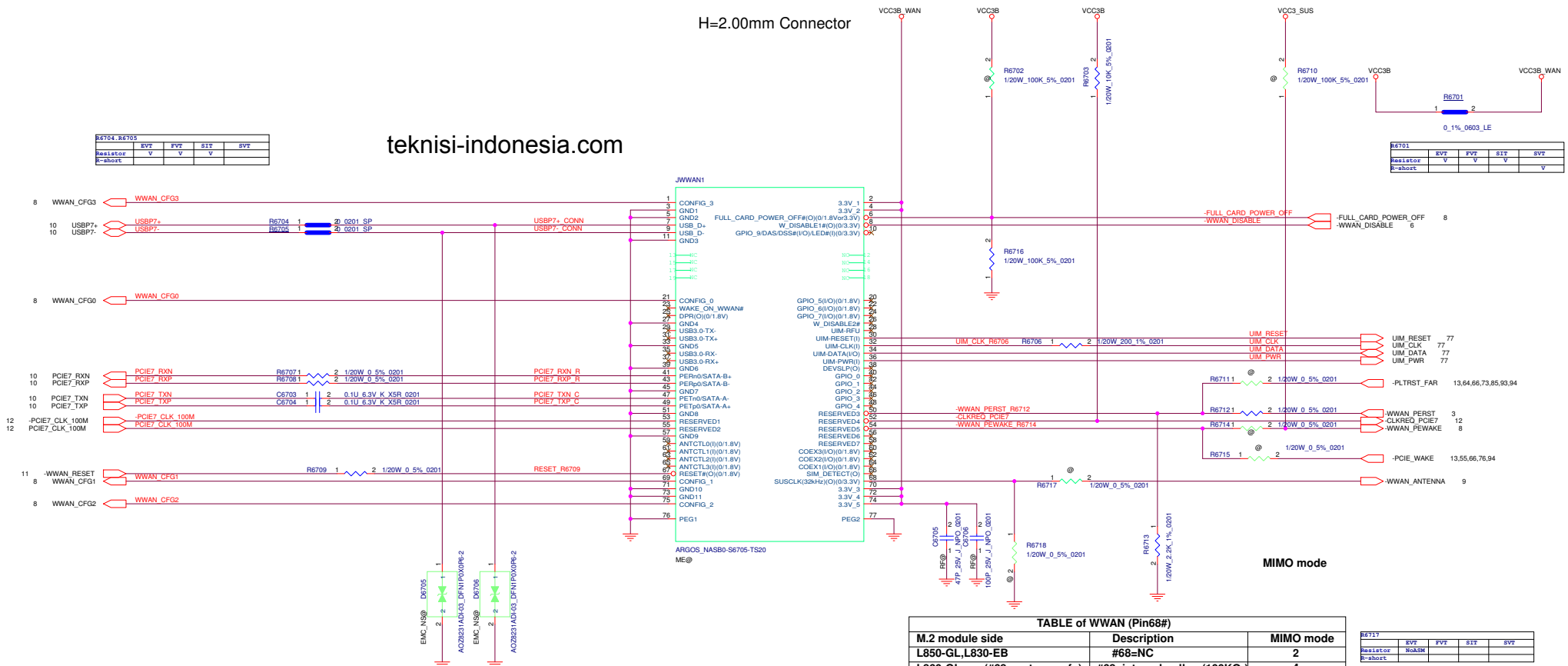
M.2 Socket 2 (Key-B) for 3042 S3 WWAN

H=2.00mm Connector

R6704.R6705				
	EVT	FVT	SIT	SVT
Resistor	V	V	V	
R-short				

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R6701				
	EVT	FVT	SIT	SVT
Resistor	V	V	V	
R-short				V



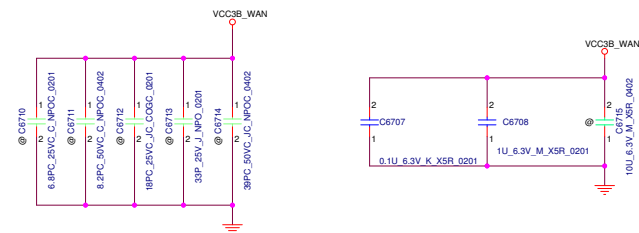
**TABLE of WWAN (Pin68#)**


M.2 module side	Description	MIMO mode
L850-GL,L830-EB	#68=NC	2
L860-GL (#68= antenna cfg)	#68=internal pull up(100KΩ)	4

R6717				
	EVT	FVT	SIT	SVT
Resistor	NoASM			
R-short				

TABLE:

State #	Module Configuration Decodes				Module Type and Main Host Interface	Port Configuration	Module
	CONFIG 0 (Pin 21)	CONFIG 3 (Pin 1)	CONFIG 2 (Pin 75)	CONFIG 1 (Pin 69)			
0	GND	GND	GND	GND	SSD - SATA	N/A	
1	GND	GND	GND	NC	SSD - PCIe	N/A	
2	GND	GND	NC	GND	WWAN - PCIe	0	
3	GND	GND	NC	NC	WWAN - PCIe	1	
4	GND	NC	GND	GND	WWAN - PCIe, USB 3.1 Gen1	0	WWAN L850
5	GND	NC	GND	NC	WWAN - PCIe, USB 3.1 Gen1	1	
6	GND	NC	NC	GND	WWAN - PCIe, USB 3.1 Gen1	2	
7	GND	NC	NC	NC	WWAN - PCIe, USB 3.1 Gen1	3	
8	NC	GND	GND	GND	WWAN - SSIC	0	WWAN L830
9	NC	GND	GND	NC	WWAN - SSIC	1	
10	NC	GND	NC	GND	WWAN - SSIC	2	
11	NC	GND	NC	NC	WWAN - SSIC	3	
12	NC	NC	GND	GND	WWAN - PCIe	2	
13	NC	NC	GND	NC	WWAN - PCIe	3	
14	NC	NC	NC	GND	WWAN - PCIe, USB 3.1 Gen1	Vendor Defined	WWAN L860
15	NC	NC	NC	NC	No Module Present	N/A	



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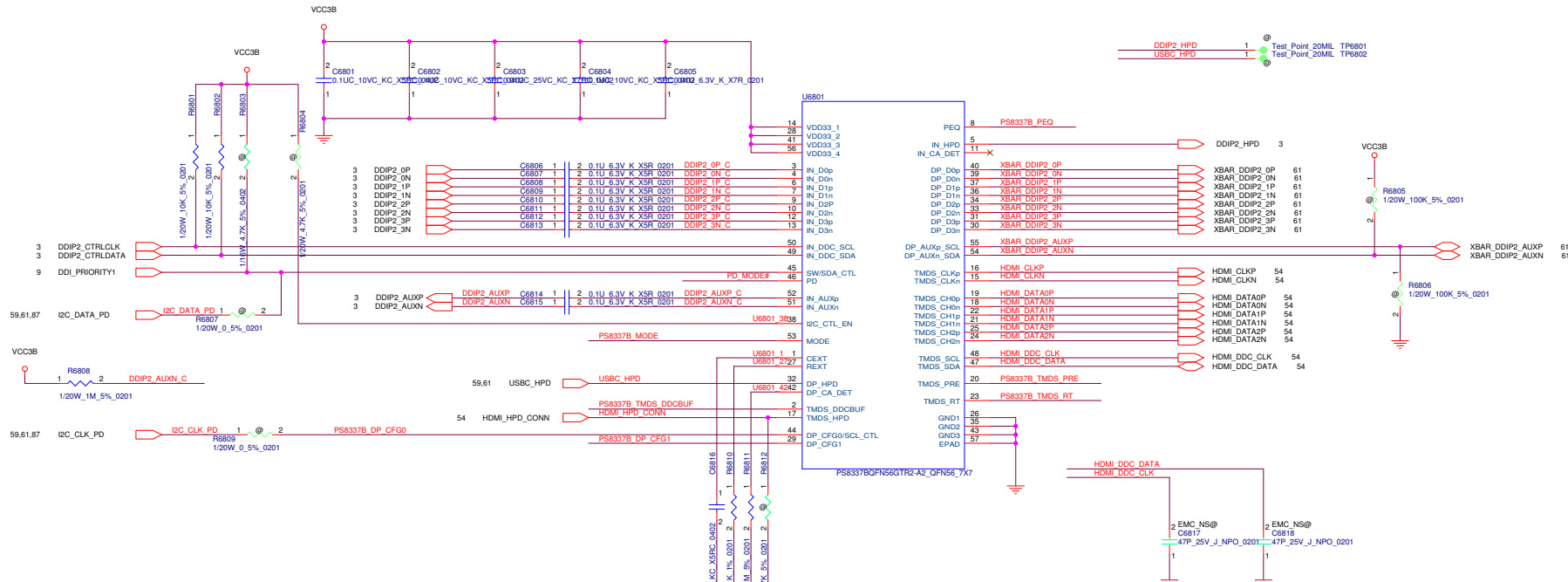
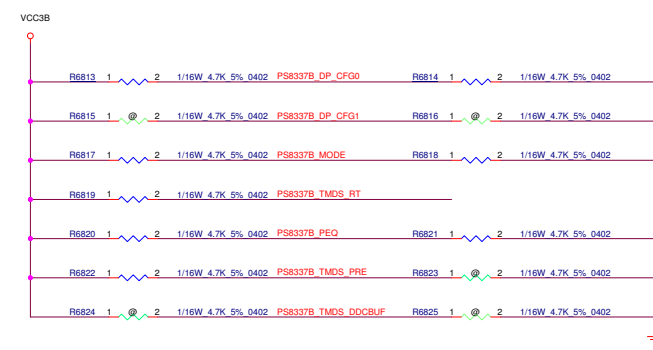
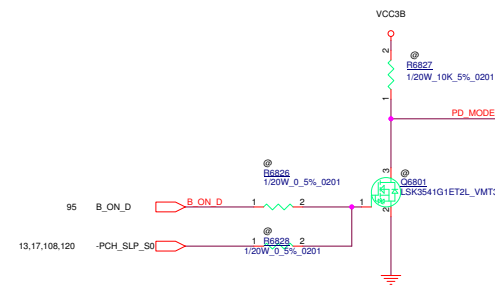


TABLE: Automatic Switching Mode (MODE=H/M)

SW(DDI_PRIORITY1)	
L	DP Port has higher priority when both ports are plugged
H	TMDS Port has higher priority when both ports are plugged

MODE =	
H	Automatic Switching mode, HDMI ID Disabled
M	Automatic Switching mode, HDMI ID Enabled
L	Control Switching mode, HDMI ID Disabled



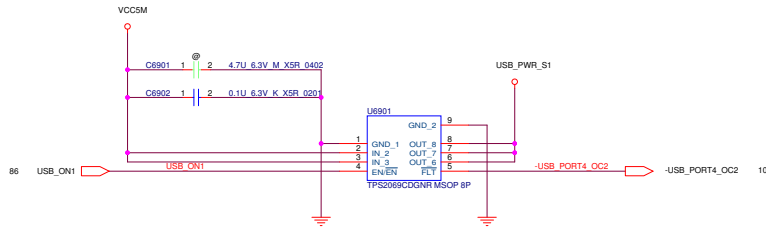
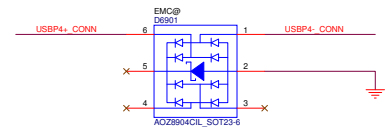
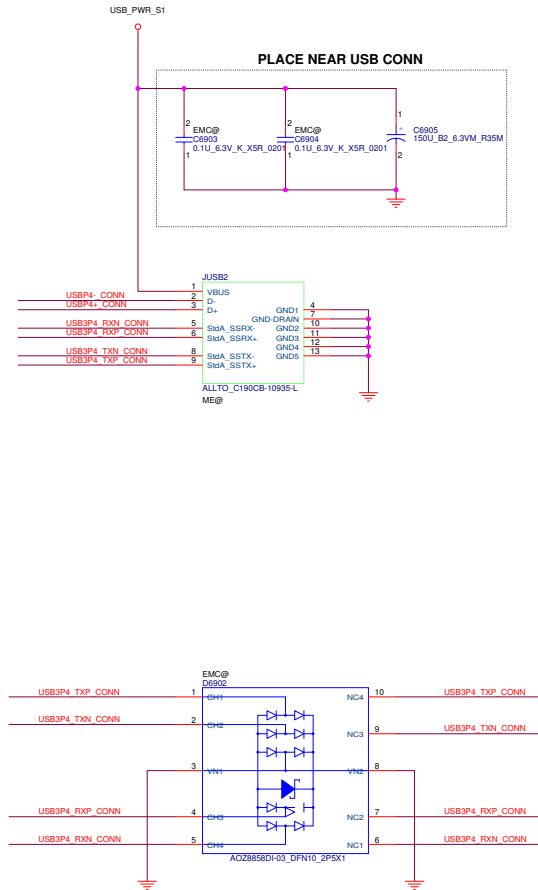
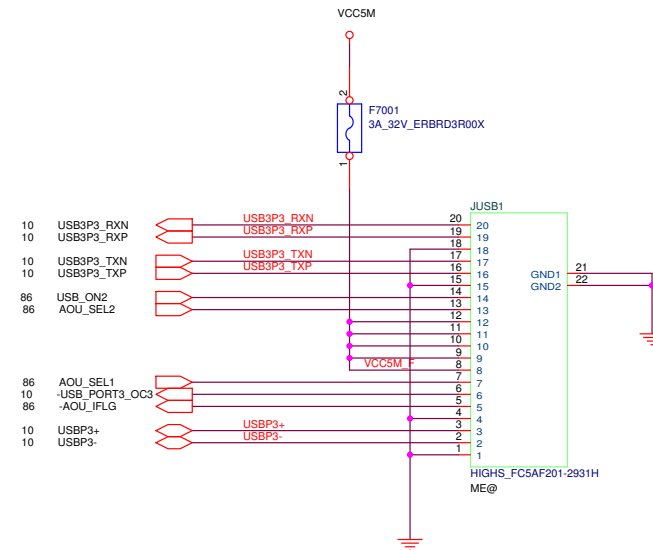



TABLE of USB3.0 Single (U6901)		
Vendor	P/N	LCFC P/N
TI	TPS2069CDGMR	SA00005TE00
Rohm	BD82032FVJ-GE2	SA000084S00

R6911, R6917, R6918, R6922, R6923, R6924				
SIZE	SVF	PVF	SVF	SVF
Resistor	V			






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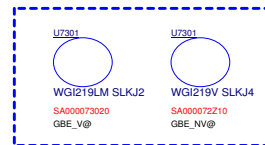
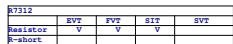
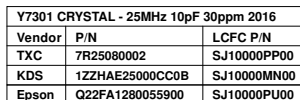




TABLE		
0201	vPro Capability	
GbE PHY	Yes	No
U7301	Jacksonville-LM	Jacksonville-V

↑  
LOGIC


SKU	Description	LCFC P/N
vPRO	WGI219LM SLKJ2	SA000073020
non-vPRO	WGI219V SLKJ4	SA000072210

R7314				
	EVT	FVT	SIT	SVT
Resistor	V	V	V	
R-short				V




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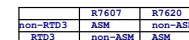
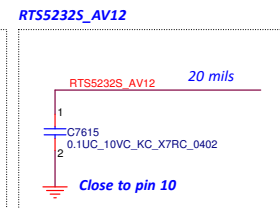
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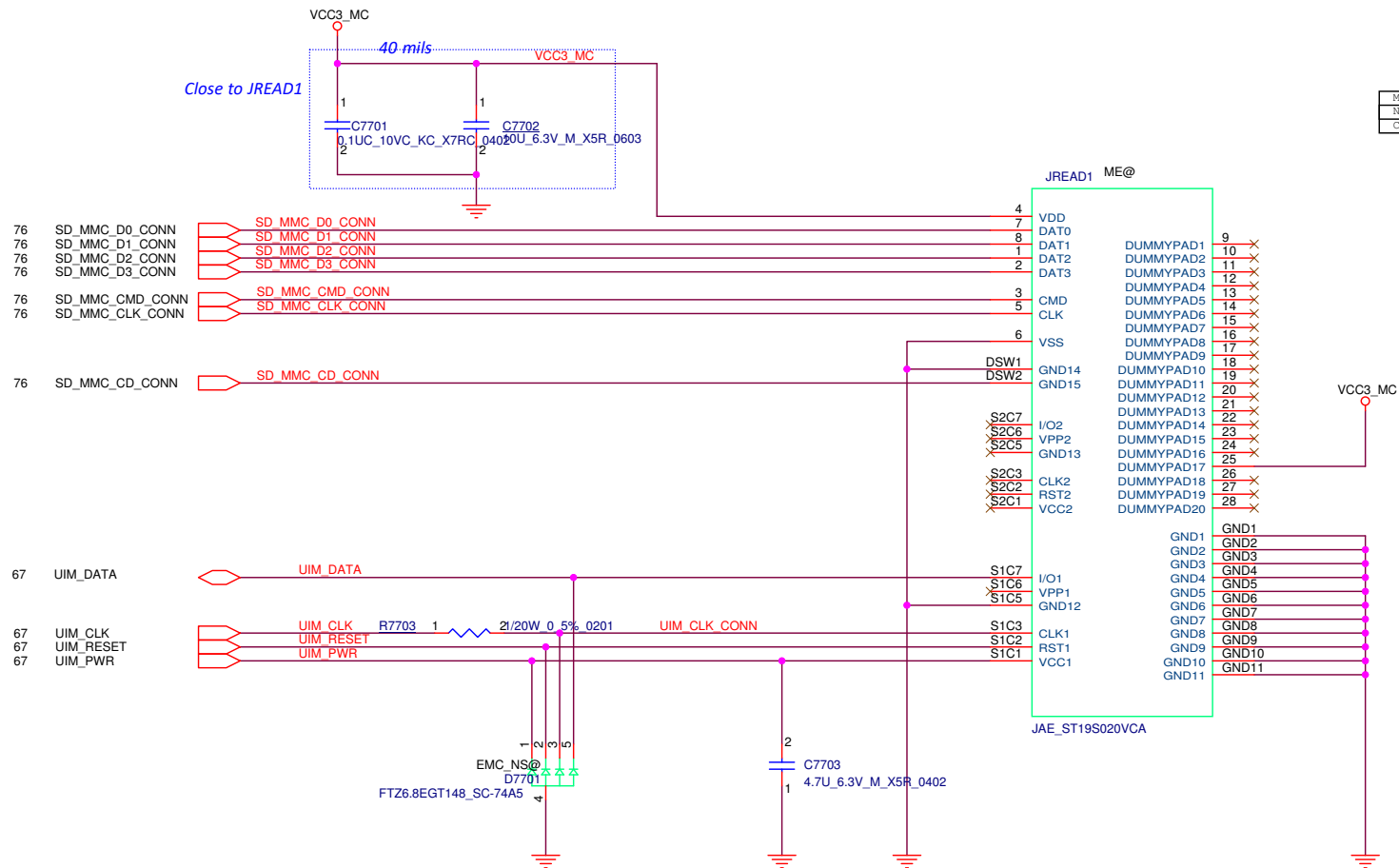
R7608,R7609,R7611,R7612,R7613,R7617				
	EVT	FVT	SIT	SVT
Resistor	V	V	V	
R-short				V

Part Number	Vendor
SA000077K00	RTS5232S-GR REALTEK
SA00009JG10	GL9750-OIY02 GENESYS

Title	<b><i>MEDIA CARD CONTROLLER</i></b>
-------	-------------------------------------

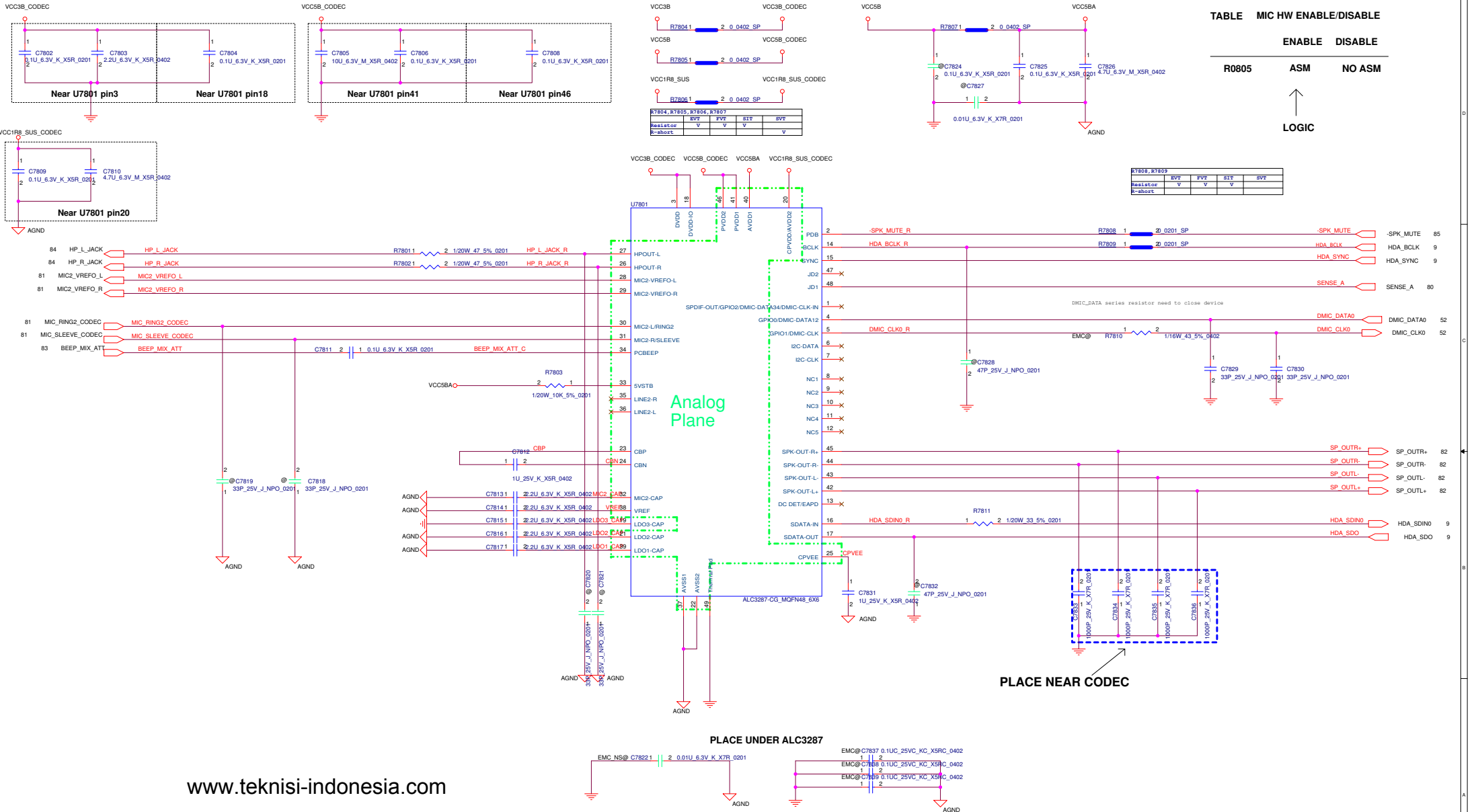


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Title		Rev	
MEDIA CARD CONTROLLER		0.1	
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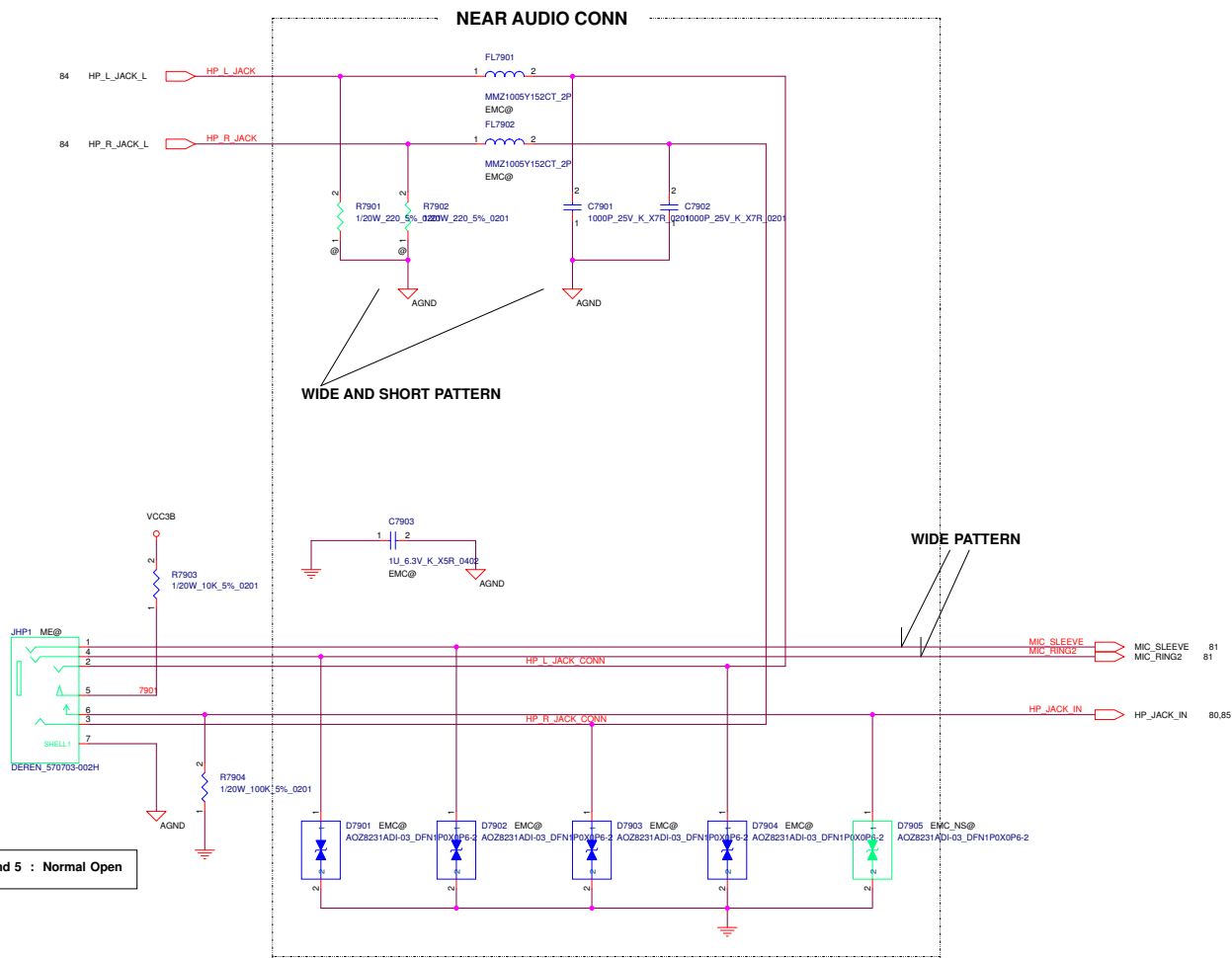
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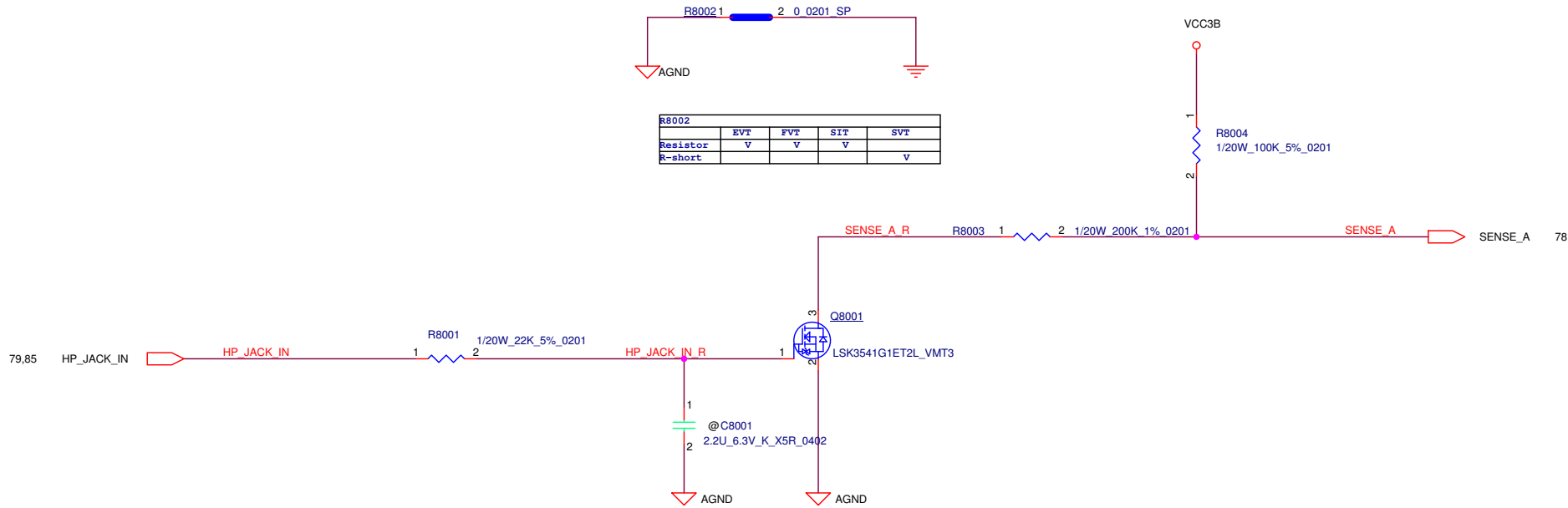
TABLE MIC HW ENABLE/DISABLE

	ENABLE	DISABLE
R0805	ASM	NO ASM
	↑ LOGIC	

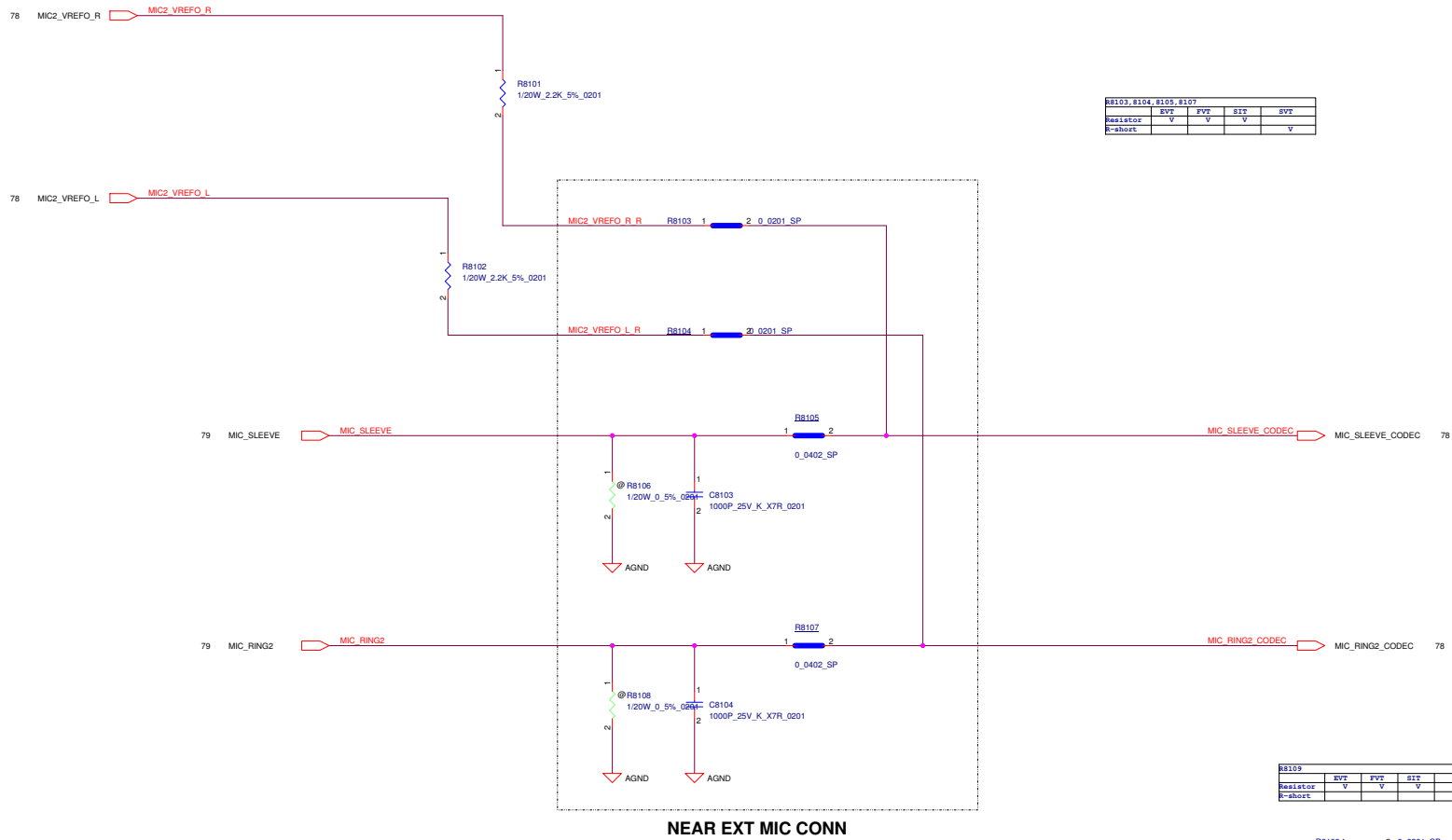
R7805, R7809	SVT	PVT	STP	SVT
Resistor	V	V	V	V
Short				

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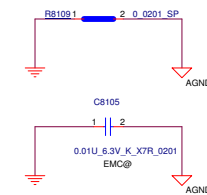


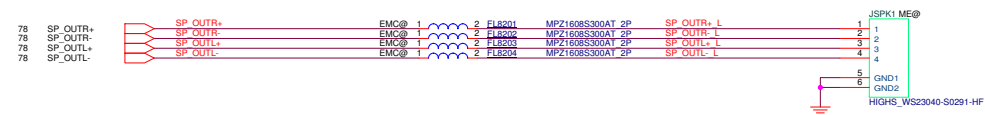




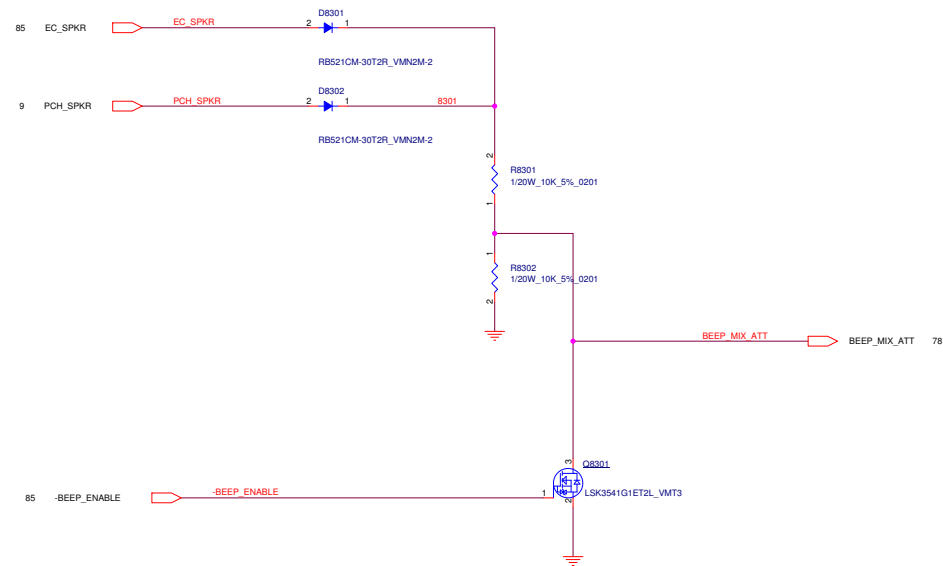
R8103, R8104, R8105, R8107	SVF	FVF	STV	SVF
Resistor	V	V	V	V
R-shoot				V

R8109	SVF	FVF	STV	SVF
Resistor	V	V	V	V
R-shoot				V





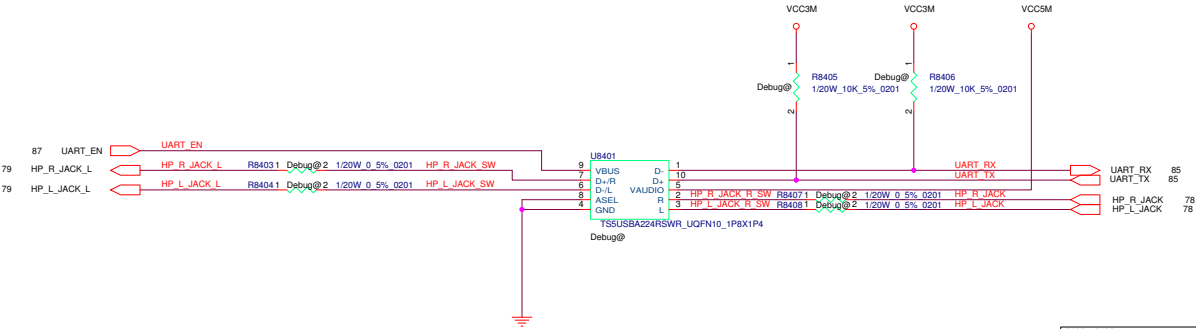
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				125	



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Date:	Monday, February 18, 2020	Sheet	83	of	125

TABLE:

Mode	Audio	UART
UART_EN	L	H

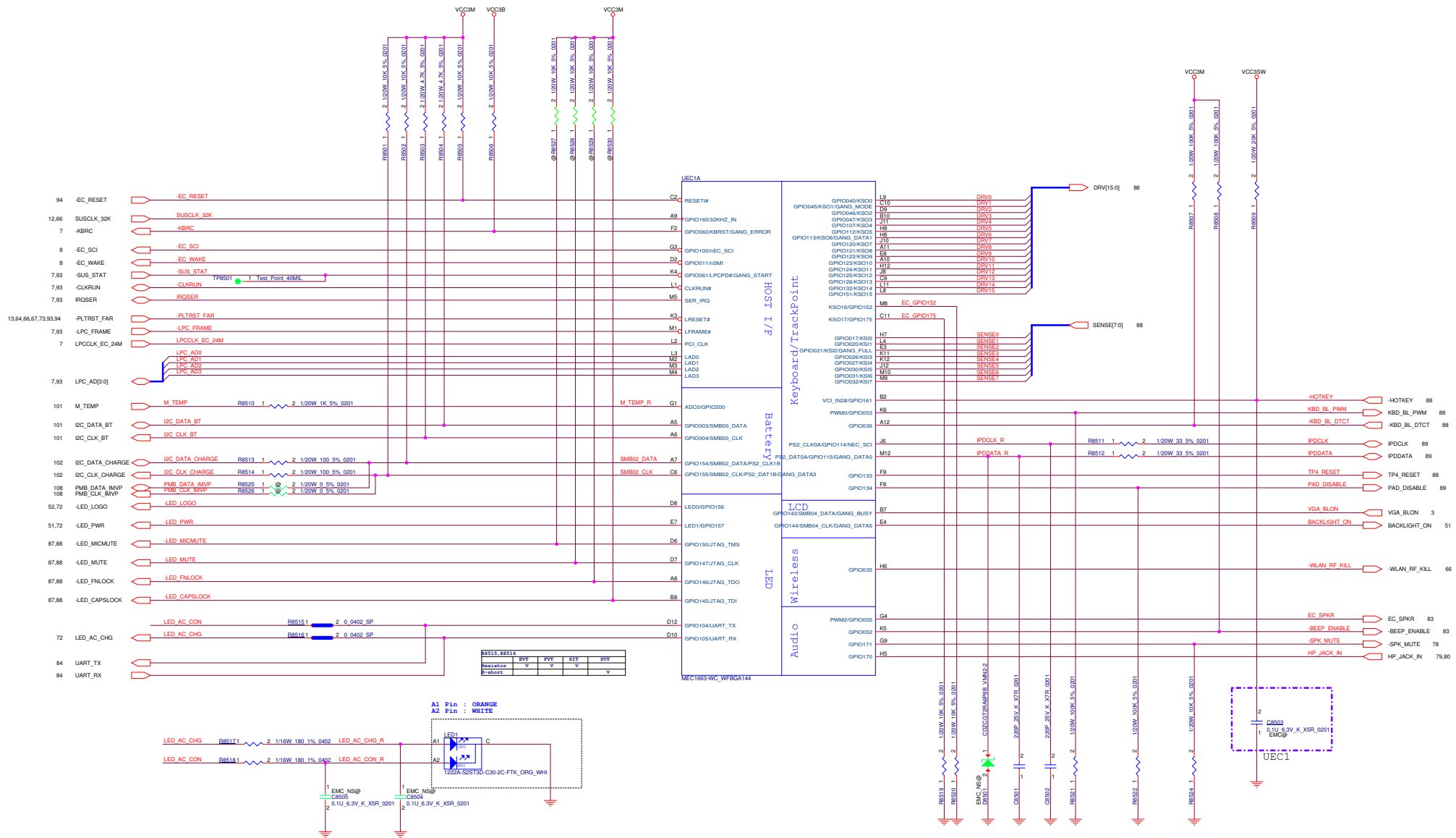


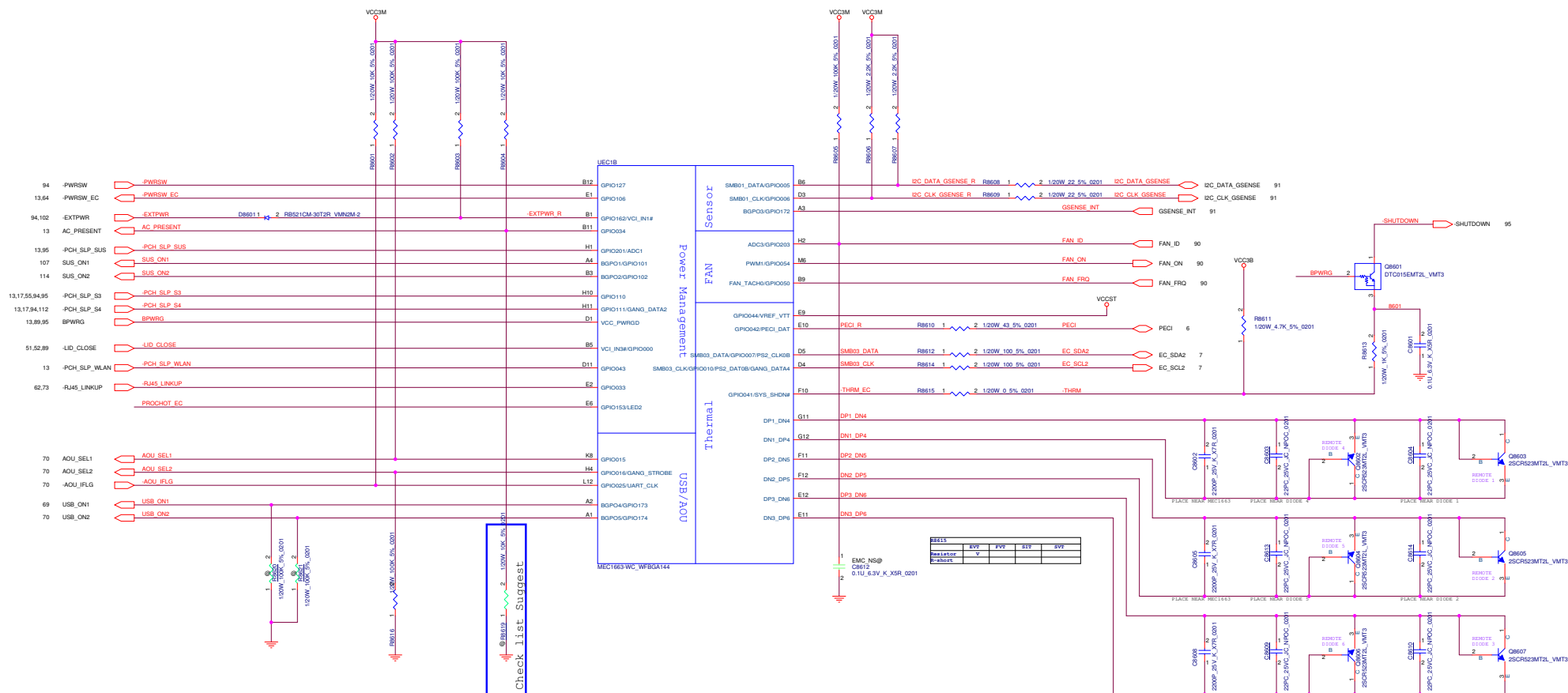
HP\_R\_JACK\_L R8409 2 SS@ 1 1/20W 0.5% 0201 HP\_R\_JACK\_L RR R8401 2 SS@ 1 1/20W 0.5% 0201 HP\_R\_JACK  
HP\_L\_JACK\_L R8410 2 SS@ 1 1/20W 0.5% 0201 HP\_L\_JACK\_L RR R8402 2 SS@ 1 1/20W 0.5% 0201 HP\_L\_JACK

R8407, R8408	SVT	PVT	STT	SVT
Resistor	V			
R-short				

R8403, R8404	SVT	PVT	STT	SVT
Resistor	V			
R-short				

R8401, R8402	SVT	PVT	STT	SVT
Resistor	V			
R-short				

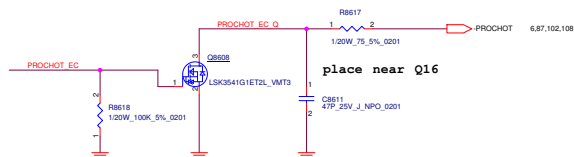


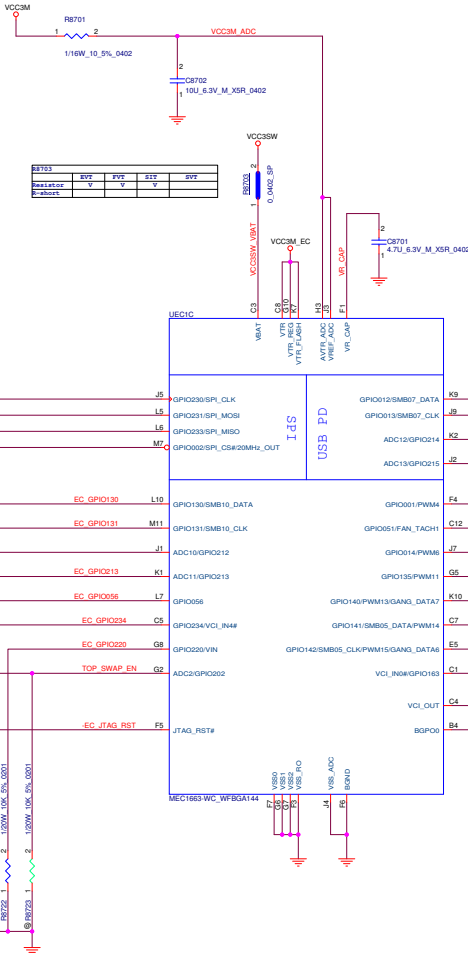
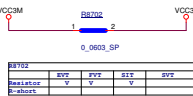


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TABLE

Sensor	Device	Placed on
DIODE0	EC internal	TOP
DIODE1	CPU DC/DC	BOTTOM
DIODE2	Charger	BOTTOM
DIODE3	FAN	BOTTOM
DIODE4	SSD	BOTTOM
DIODE5	WLAN/WiGig	BOTTOM
DIODE6	DDR4	BOTTOM



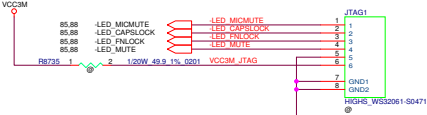
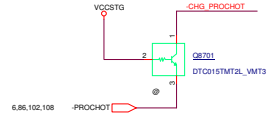


- 94 ECSP\_CLK
- 94 ECSP\_MOSI
- 94 ECSP\_MISO
- 94 ECSP\_SS

3.51 LCD\_SELF\_TEST\_ON

9 TOP\_SWAP\_EN

EC\_JTAG\_RST



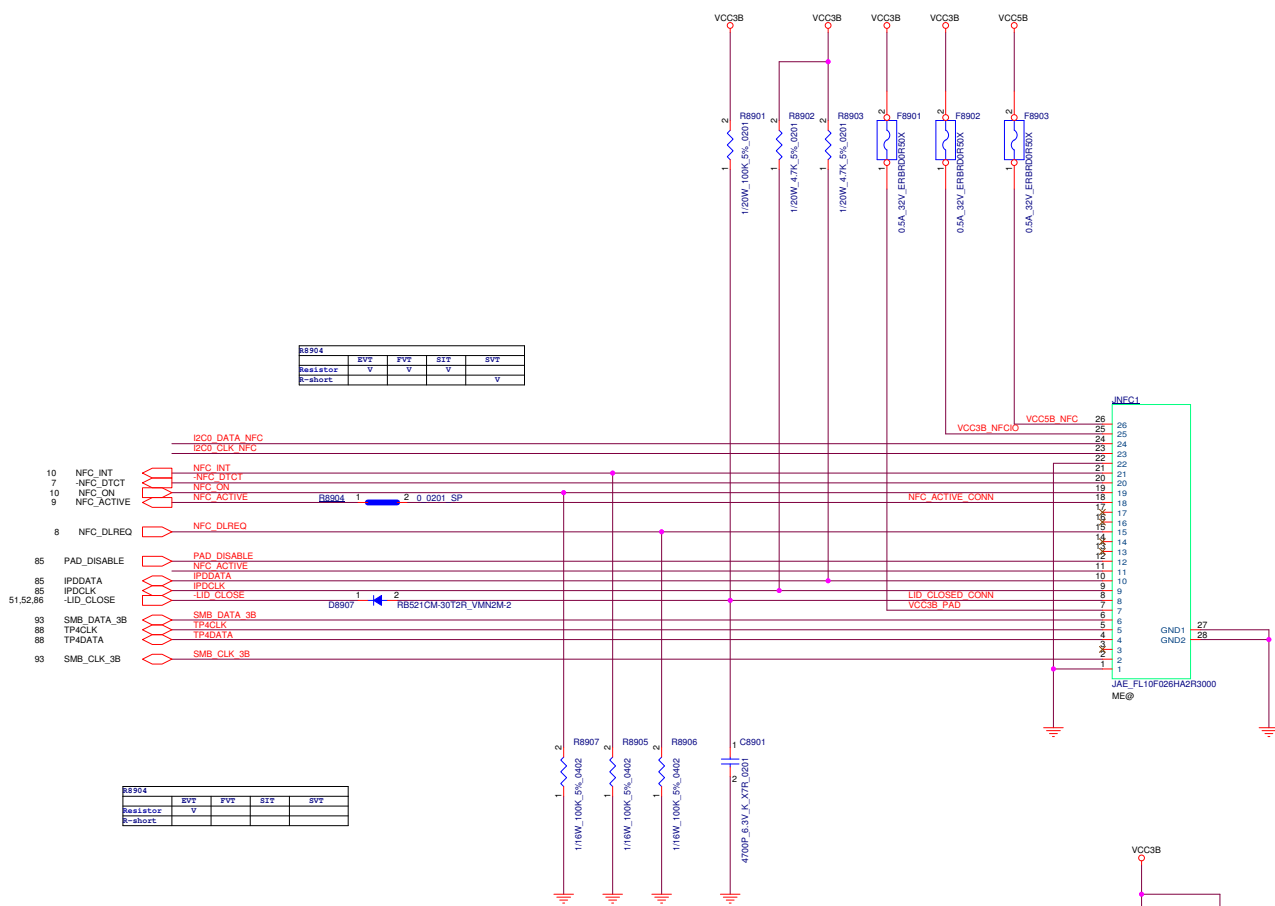
JTAG Debug Port		
	Enable	Disable
R8714	ASM	NO_ASM
R8715	NO_ASM	ASM
R8735	ASM	NO_ASM
R8527	ASM	NO_ASM
R8530	ASM	NO_ASM
R8529	ASM	NO_ASM
R8528	ASM	NO_ASM

Check list Suggest

H: DRIFT  
L: JAZZ/SIDEWIPE







R8904	SVT	FVT	SVT	SVT
Resistor	V	V	V	V
R-short				

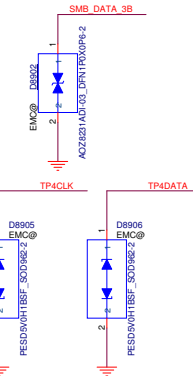
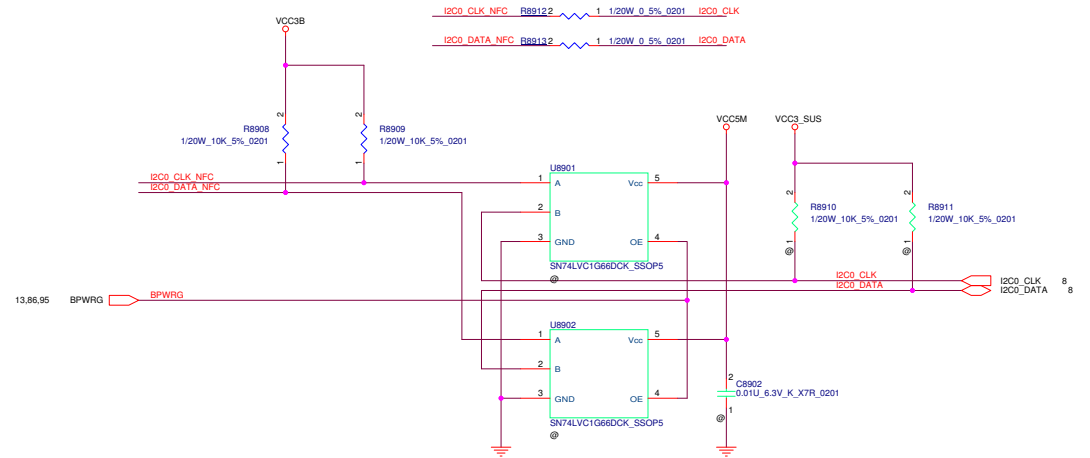


TABLE of U8901/U8902		
Vendor	P/N	LCFC P/N
TI	SN74LVC1G66DCK	SA00005BE0J
NXP	74LVC1G66GW	SA00007KS00
ONsemi	MC74VHC1G66DFT2G	SA00008JQ00

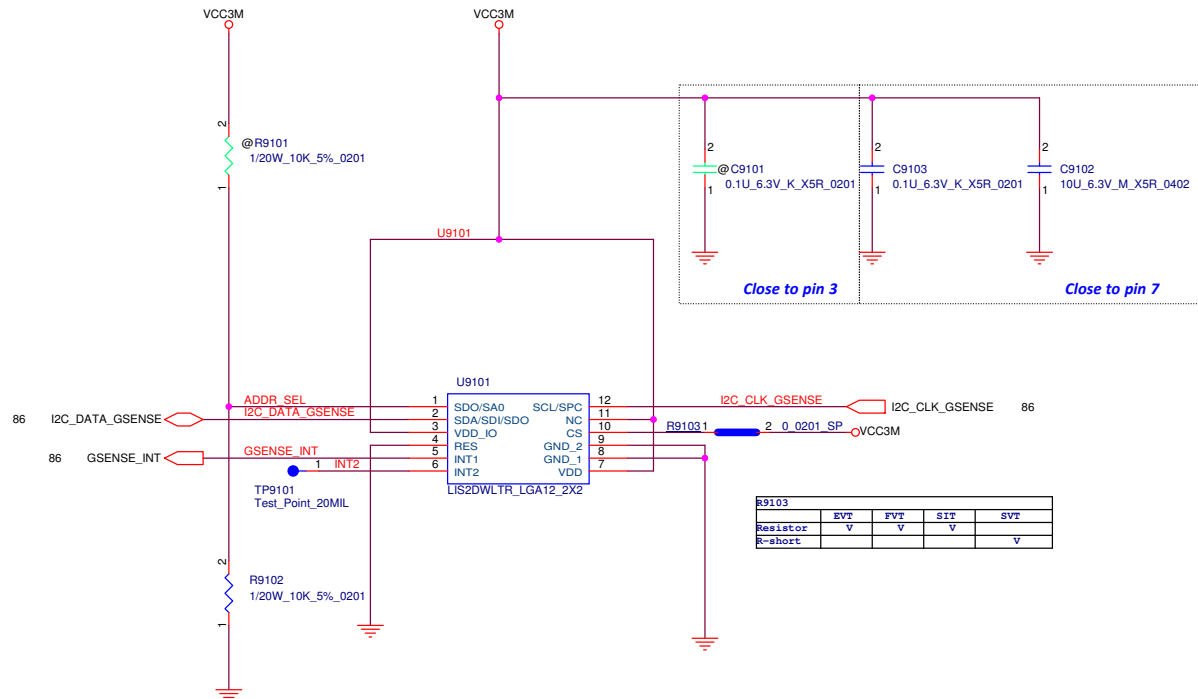





HDD Support	VCC3M
SSD Only	VCC3B

P/N	ADDR_SEL	Address
LIS2DWLTR	H L	32h (W) & 33h (R) 30h (W) & 31h (R)
KX022-1020	H L	3Eh (W) & 3Fh (R) 3Ch (W) & 3Dh (R)

TABLE of G-Sensor (U9101)		
Vendor	P/N	LCFC P/N
ST	LIS2DWLTR	SA00009AQ00
Kionix	KX022-1020	SA000081E00



R9103				
	EVT	FVT	SIT	SVT
Resistor	V	V	V	
R-short				V

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				<small>Sheet</small> 92 of 125	
				<small>Rev</small> 0.1	



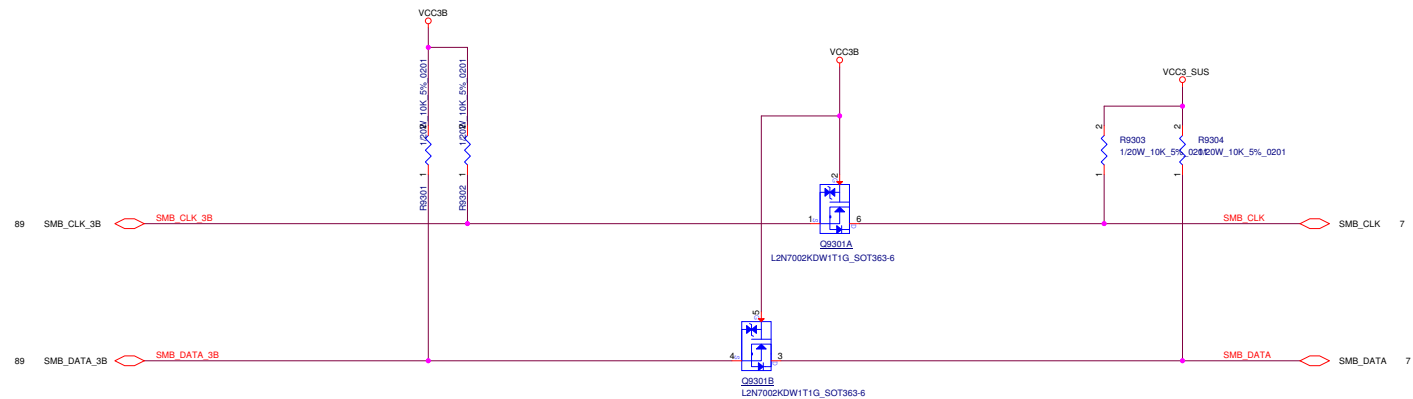
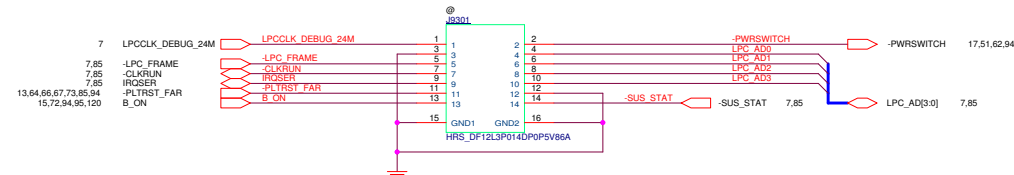
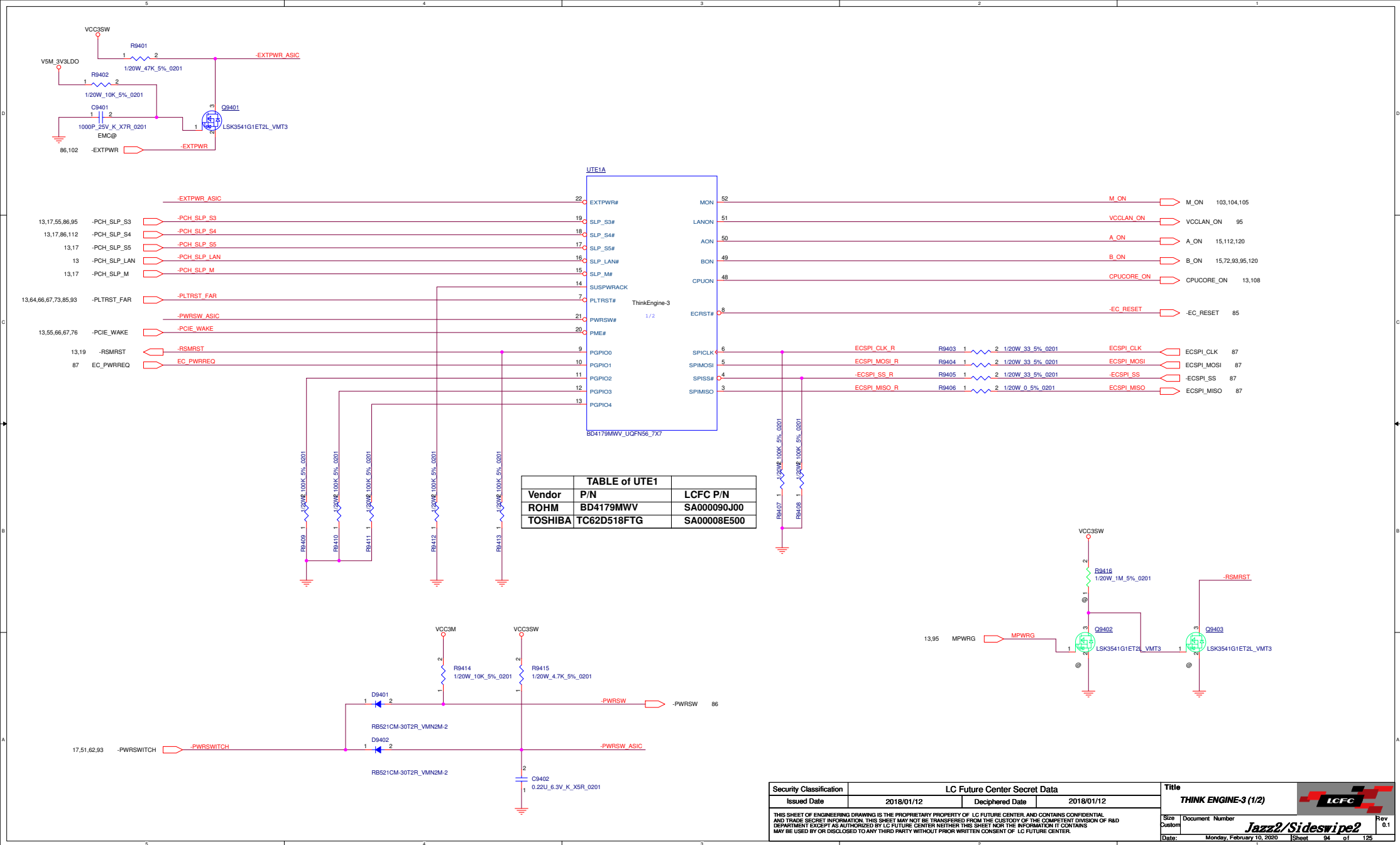


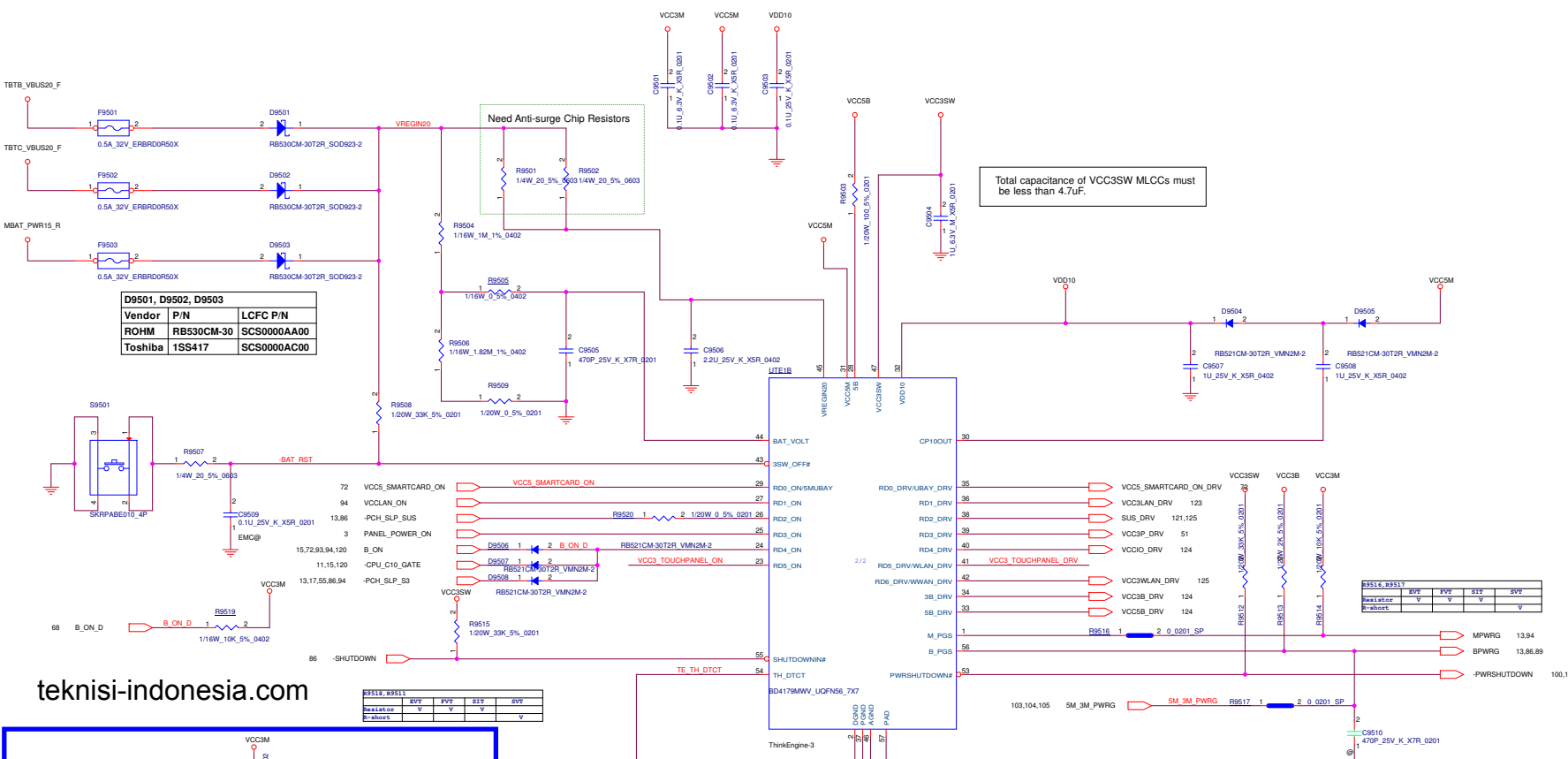
TABLE of U9301/U9302		
Vendor	P/N	LCFC P/N
TI	SN74LVC1G66DCK	SA00005BE0J
NXP	74LVC1G66GW	SA00007KS00
ONsemi	MC74VHC1G66DFT2G	SA00008JQ00

TABLE		
REF DES	ENABLE	DISABLE
J5	ASM	NO_ASM
R220	ASM	NO_ASM

↑  
LOGIC







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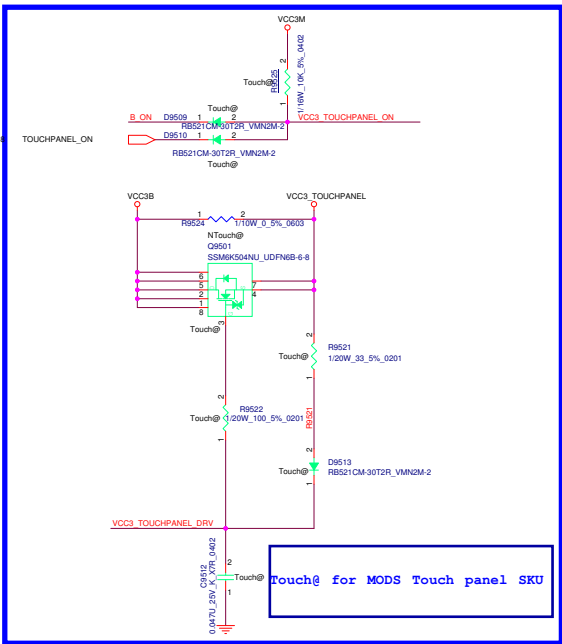



TABLE	
ID	Target
RT9501	Thunderbolt Port A VBUS FET (PQ0001,PQ0002,PQ0005,PQ0006)
RT9505	Battery Buck Charger VBUS Dual FET (PQ0201)
RT9502	Battery Boost Charger VBUS Dual FET (PQ0202)
RT9506	Battery Charger FET (PQ0203)
RT9503	Battery Charger FET (PQ0101)
RT9507	VCCCPUCORE Dr MOS Phase2 (PU0902)
RT9504	VCCCPUCORE Dr MOS Phase1 (PU0901)
RT9508	VCCGFXCORE_1 (PU1001)
RT9509	CPU Die (UCPU1)


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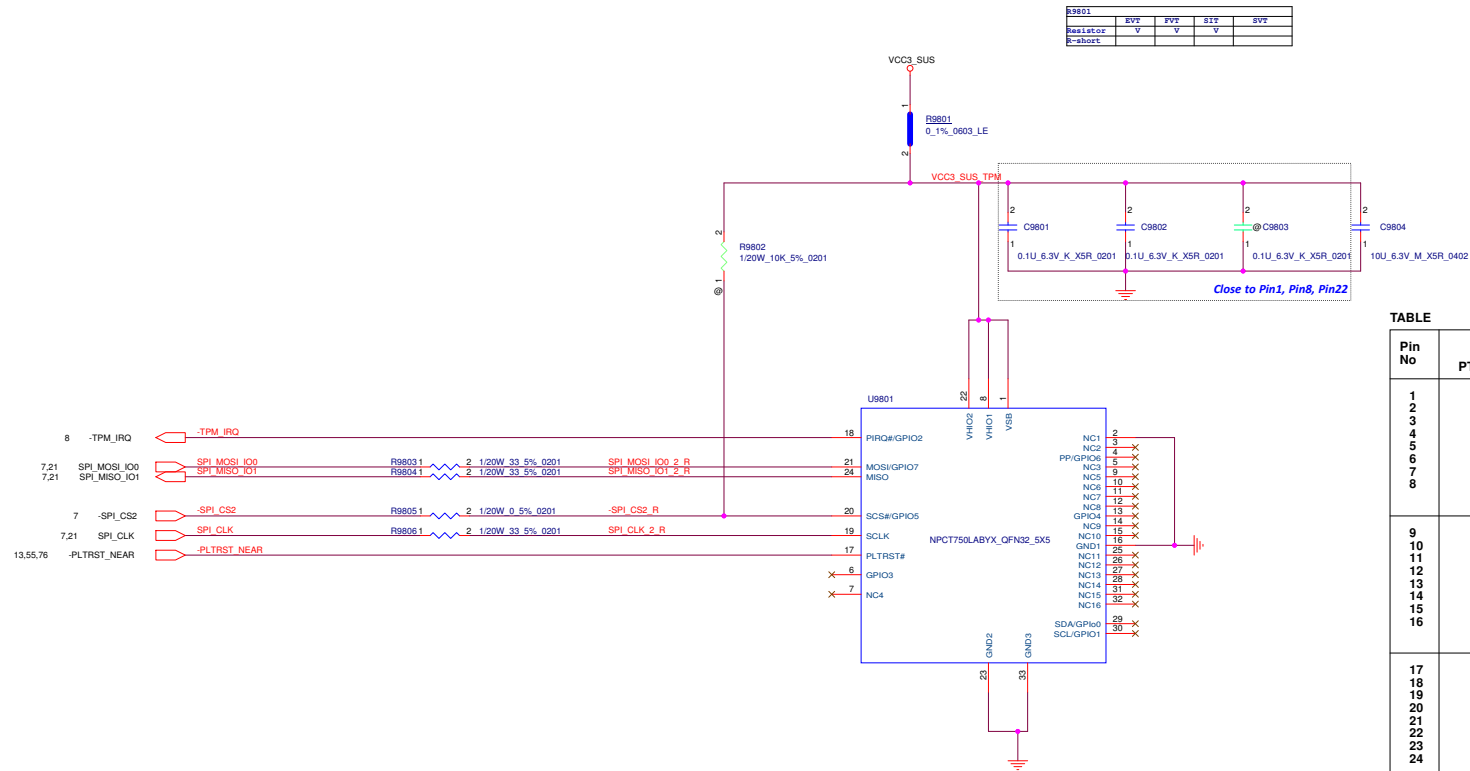


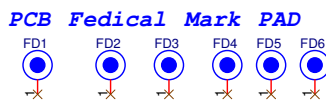
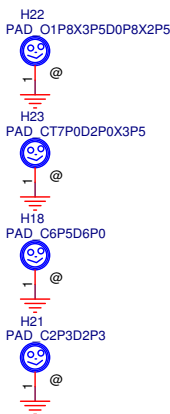
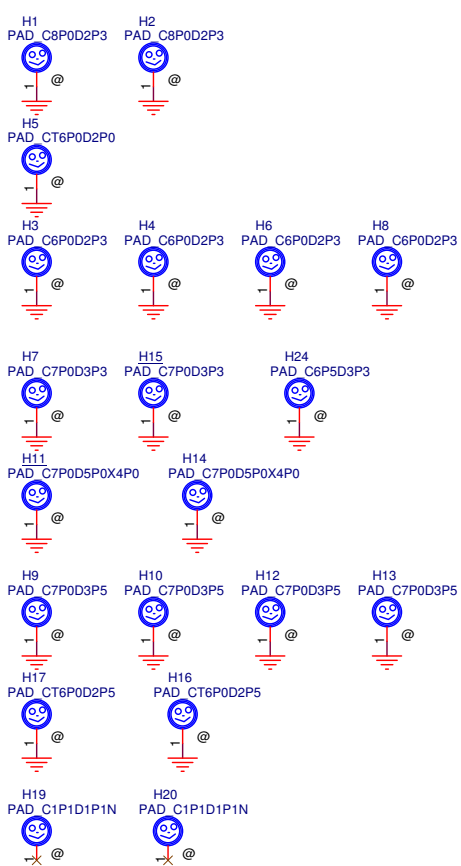
TABLE of TPM (U9801)		
Vendor	P/N	LCFC P/N
ST Micro	ST33HTPH2E32AHC0	SA0000AB710
Nuvoton	NPCT750LABYX	SA00008KS20

TABLE

Pin No	TCG PTP Spec (v38)	Nuvoton NPCT750LABYX	ST Micro ST33HTPH2E32AHC0
1	VDD	VS0	NC
2	GND	NC	GND
3	NC	NC	NC
4	GPIO	GPIO/PP	PP
5	NC	NC	NC
6	GPIO	GPIO3	NC
7	GPIO	NC	GPIO
8	VDD	VH0	NC
9	NC	NC	NC
10	NC	NC	NC
11	NC	NC	NC
12	NC	NC	NC
13	GPIO	GPIO4	NC
14	NC	NC	NC
15	NC	NC	NC
16	GND	GND	NC
17	SPI_RST#	RST#	SPI_RST#
18	SPI_PIRQ#	PIRQ#/GPIO2	SPI_PIRQ#
19	SPI_CLK	SCLK	SPI_CLK
20	SPI_CS#	SCS#/GPIO5	SPI_CS#
21	MOSI	MOSI/GPIO7	MOSI
22	VDD	VH0	VPS
23	GND	GND	NC
24	MISO	MISO	MISO
25	NC	NC	NC
26	NC	NC	NC
27	NC	NC	NC
28	NC	NC	NC
29	SDA/GPIO1	SDA/GPIO1	NC
30	SDA/GPIO0	SDA/GPIO0	NC
31	NC	NC	NC
32	NC	NC	NC

U9805	SVF	SVF	SVF	SVF
Resistor	V	V	V	V
0-shoot				

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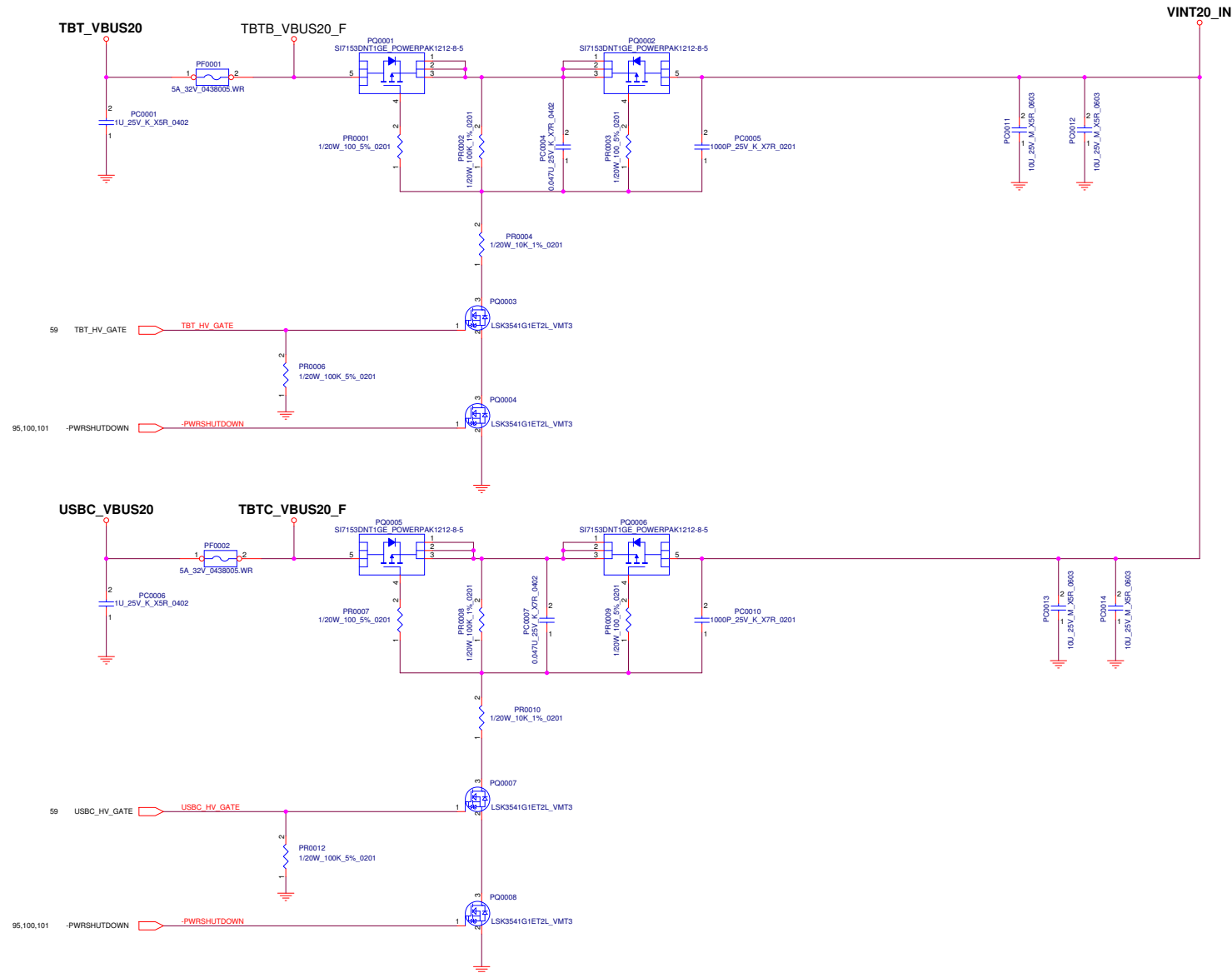
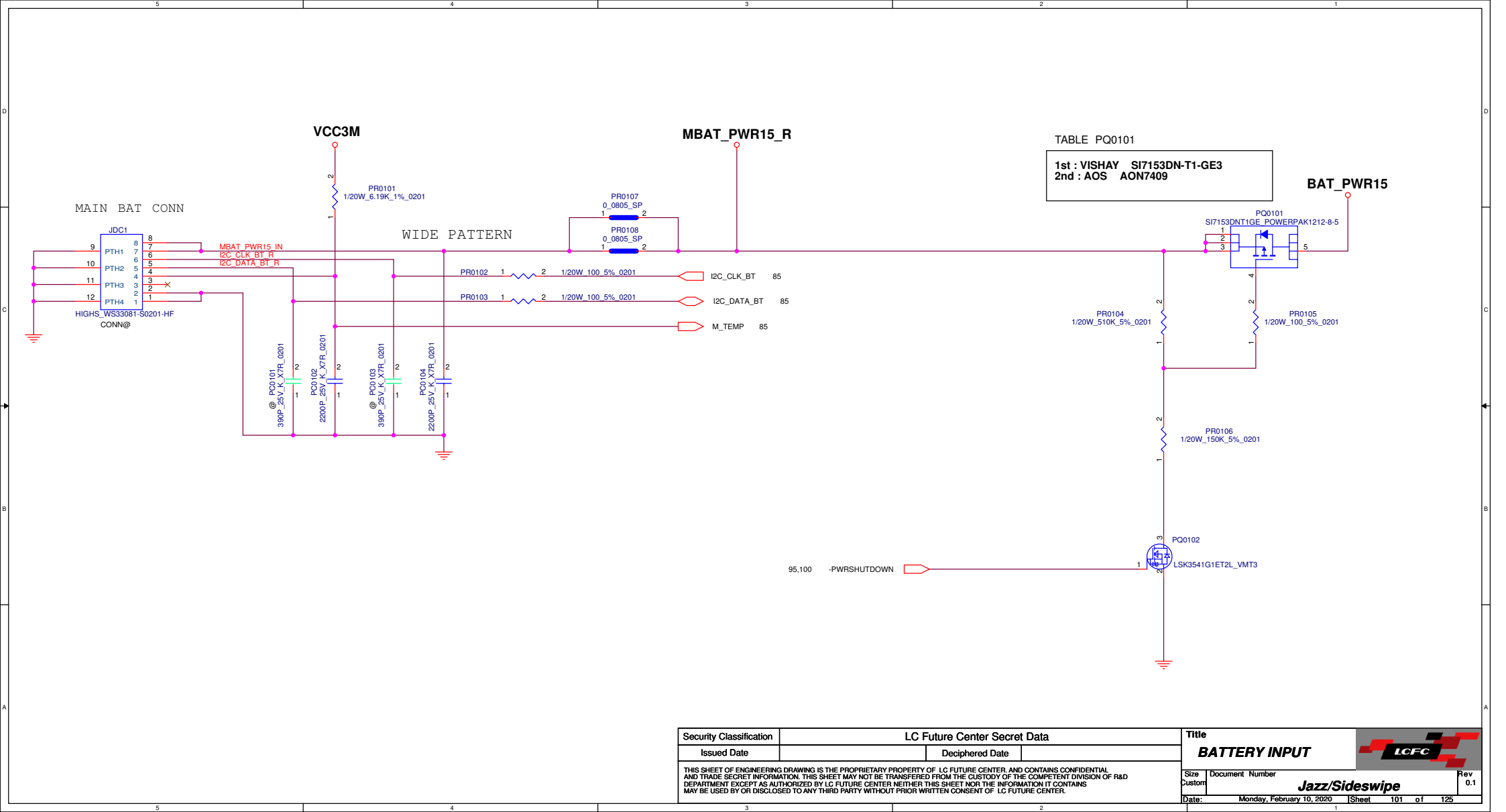
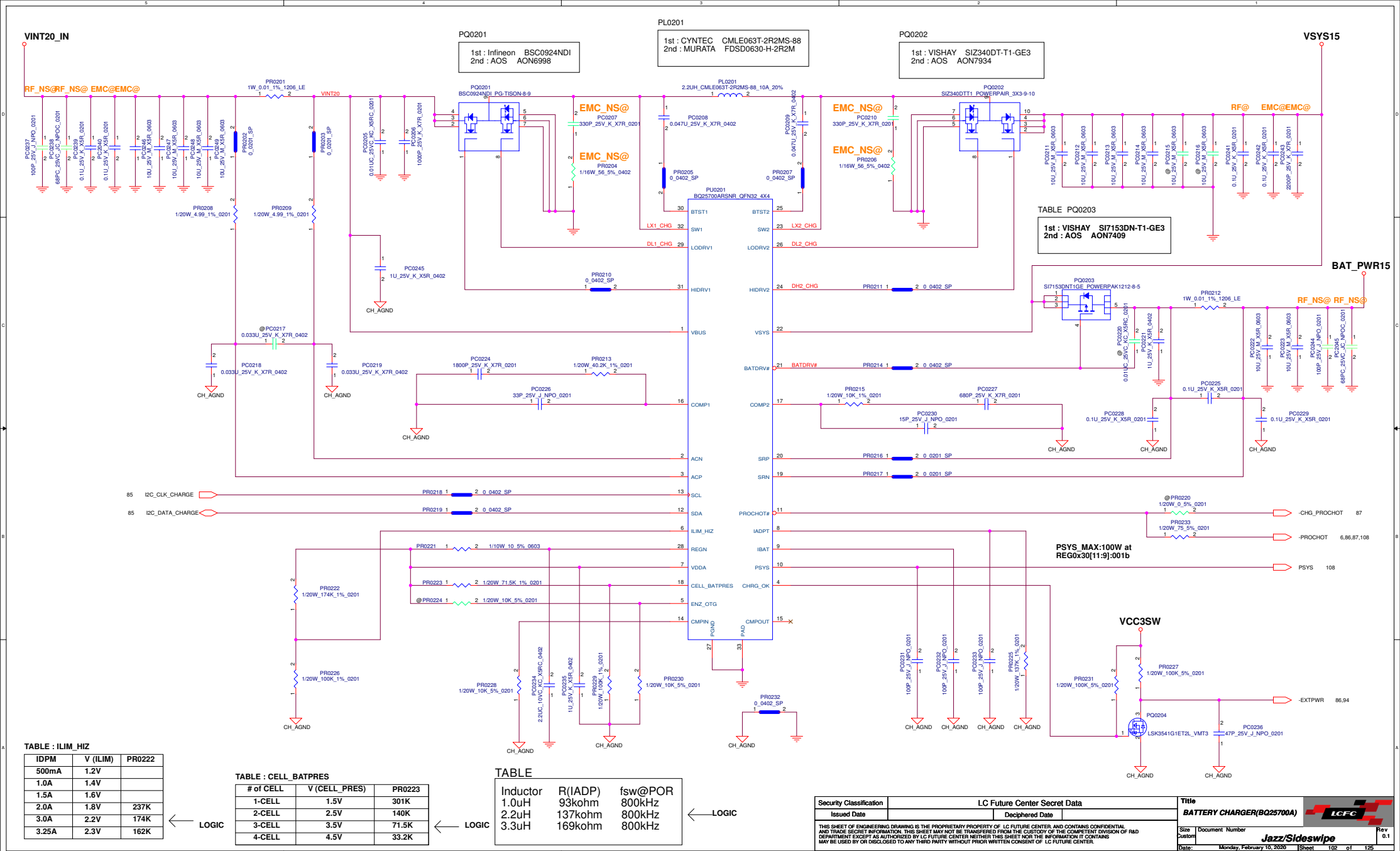
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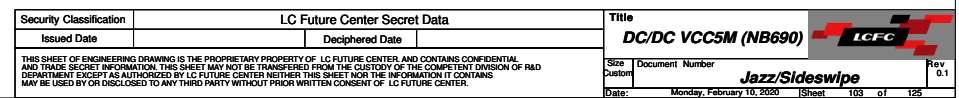
TABLE PQ0001,PQ0002,PQ0005,PQ0006

1st : VISHAY SI7153DN-T1-GE3  
2nd : AOS AON7409













VSYS15

@PJ0501  
JUMP\_43X79

RF\_NS@

EMC@

EMC@

VCC3M

MAX = 8 A  
OCP = 9.6 A


VCC3M

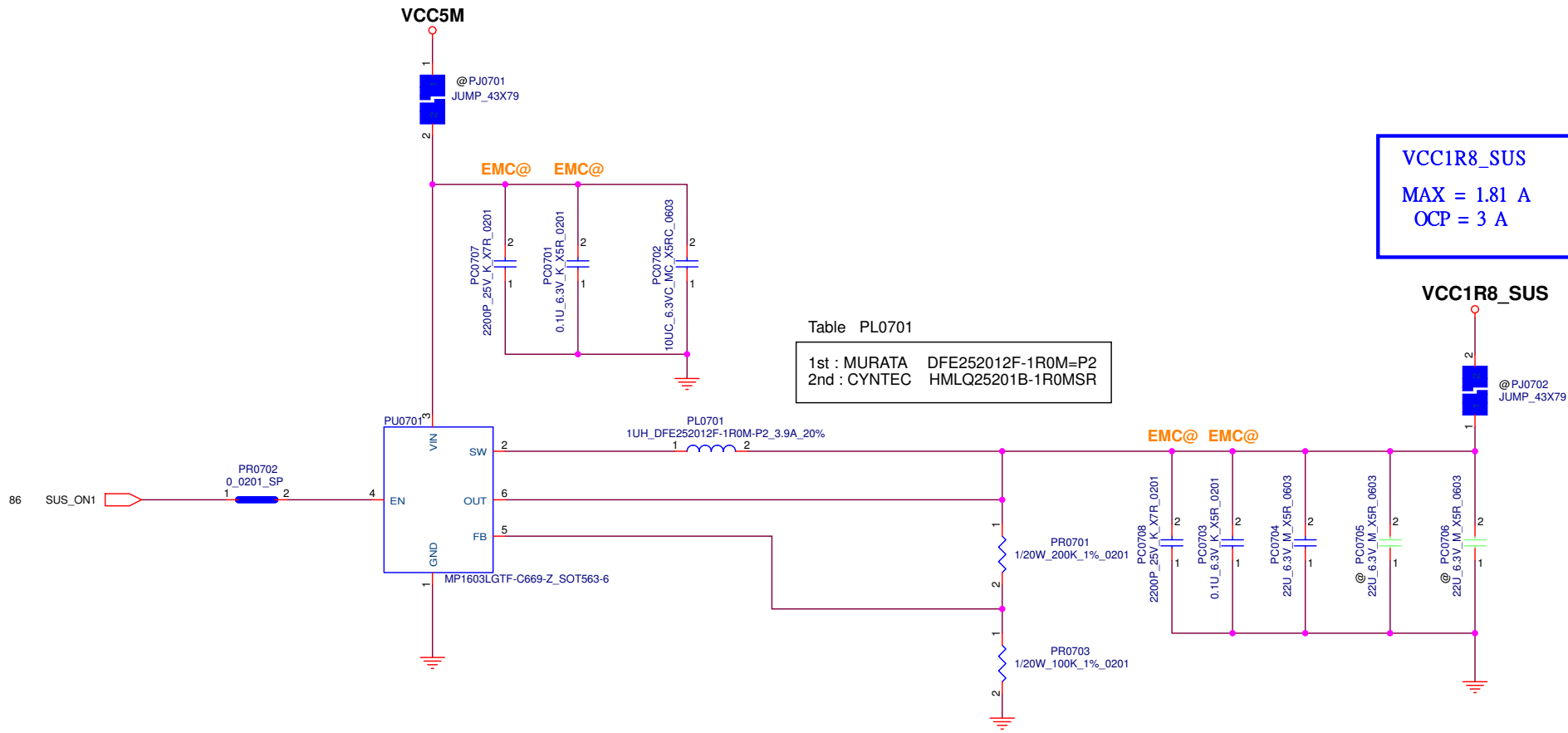
@PJ0502  
JUMP\_43X79@PJ0503  
JUMP\_43X79

Table PL0501

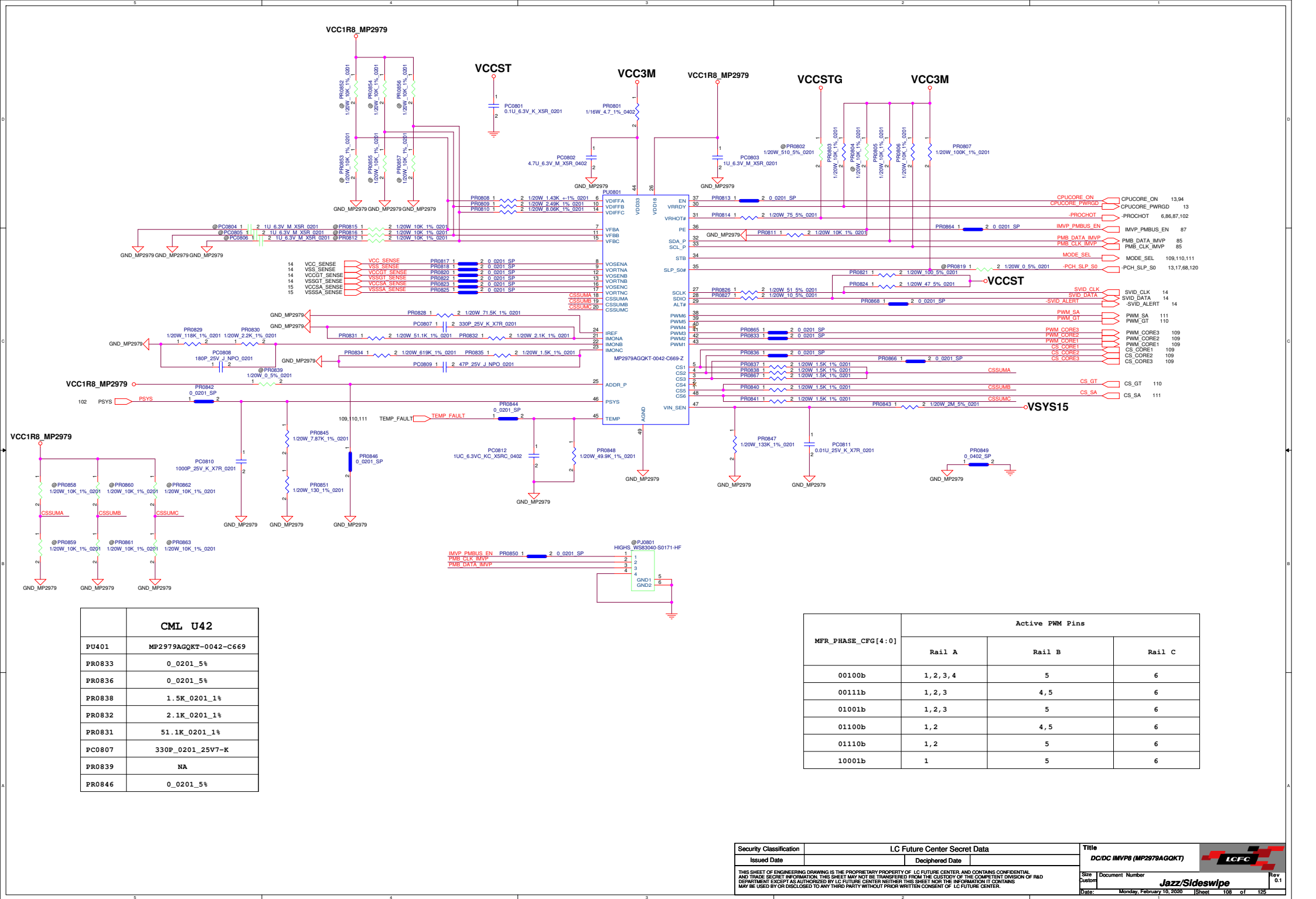
1st : CYNTEC CMLE053T-1R5MS

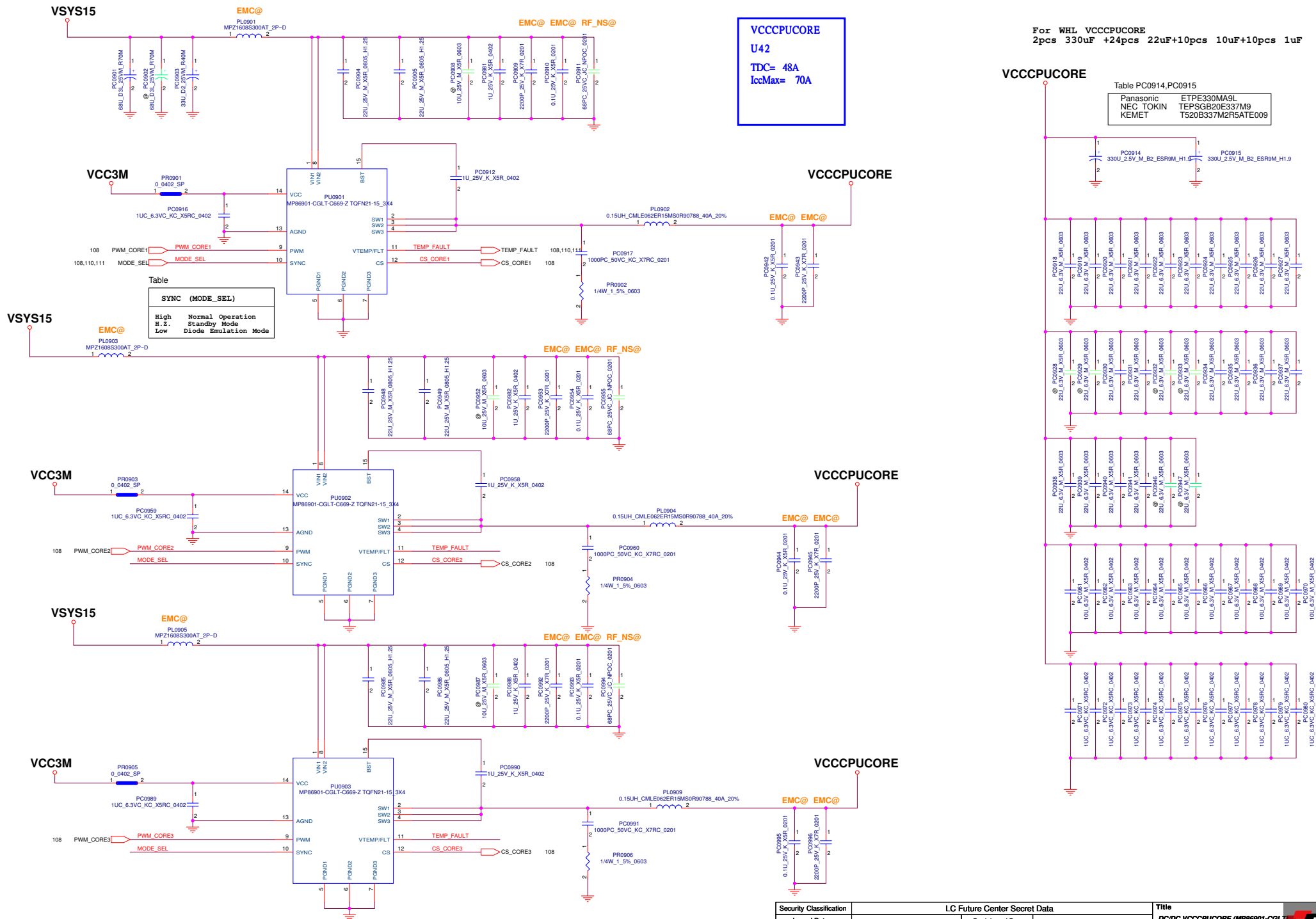
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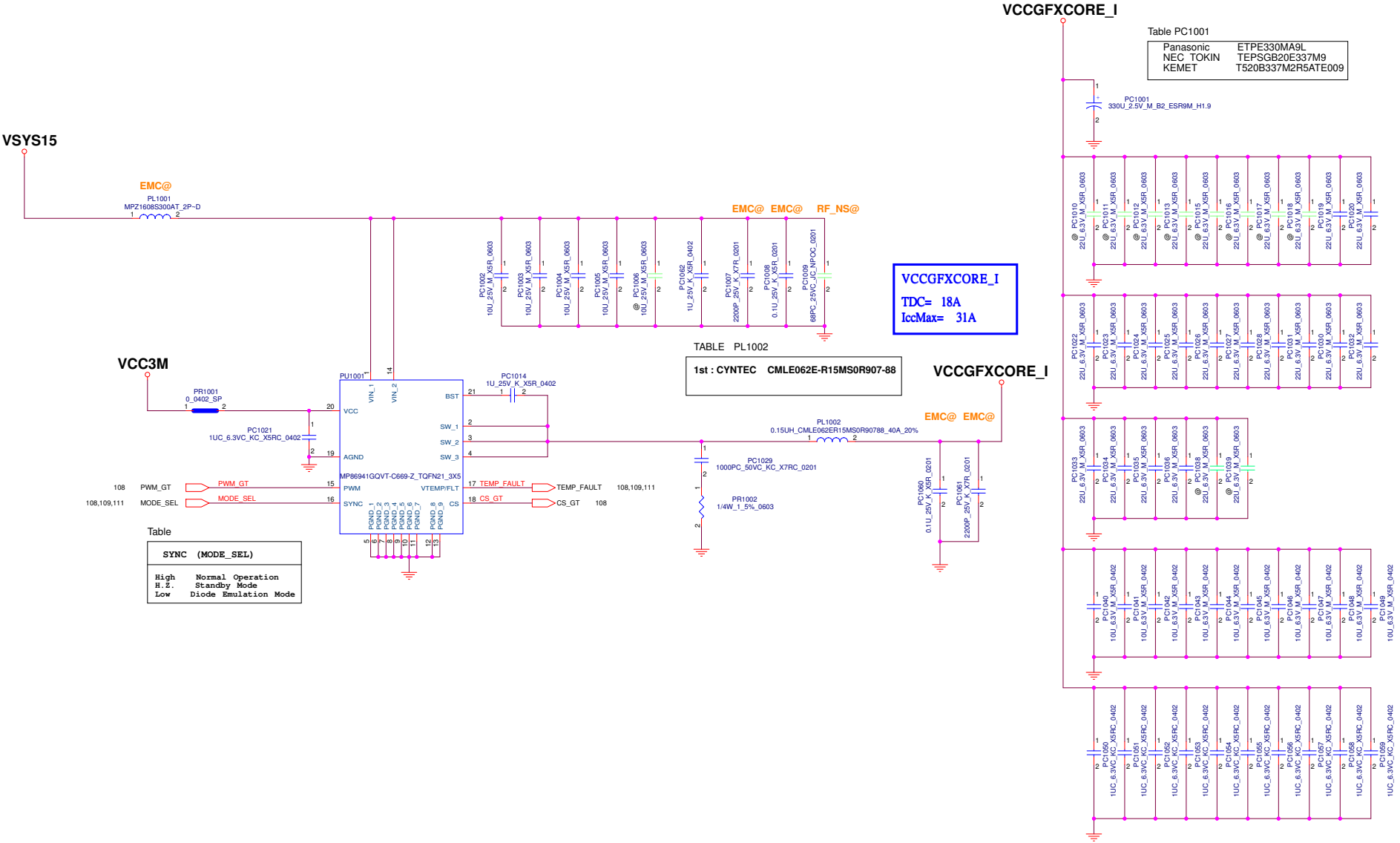


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For WHL VCCGFXCORE\_I  
1pcs 330uF +24pcs 22uF+10pcs 10uF+10pcs 1uF



VCCGFXCORE\_I  
TDC= 18A  
IccMax= 31A

TABLE PL1002  
1st : CYNTEC CMLE062E-R15MS0R907-88

Table PC1001  
Panasonic ETPE330MA9L  
NEC TOKIN TEPSGB20E337M9  
KEMET T520B337M2R5ATE009

SYNC (MODE_SEL)	
High	Normal Operation
B.Z.	Standby Mode
Low	Diode Emulation Mode

VSYS15

EMC@

PL1101  
MPZ1608S300AT\_2P-D

EMC@ EMC@ RF\_NS@

For WHL VCCSA  
8pcs 22uF+7pcs 10uF+7pcs 1uF

VCC3M

Table

SYNC (MODE_SEL)	
High	Normal Operation
H.Z.	Standby Mode
Low	Diode Emulation Mode

TABLE PL1102

CYNTEC CMLB051H-R33MS-88  
NEC-Tokin MPLCH0520LR33

VCCSA  
TDC= 4A  
IccMax= 6A

VCCSA

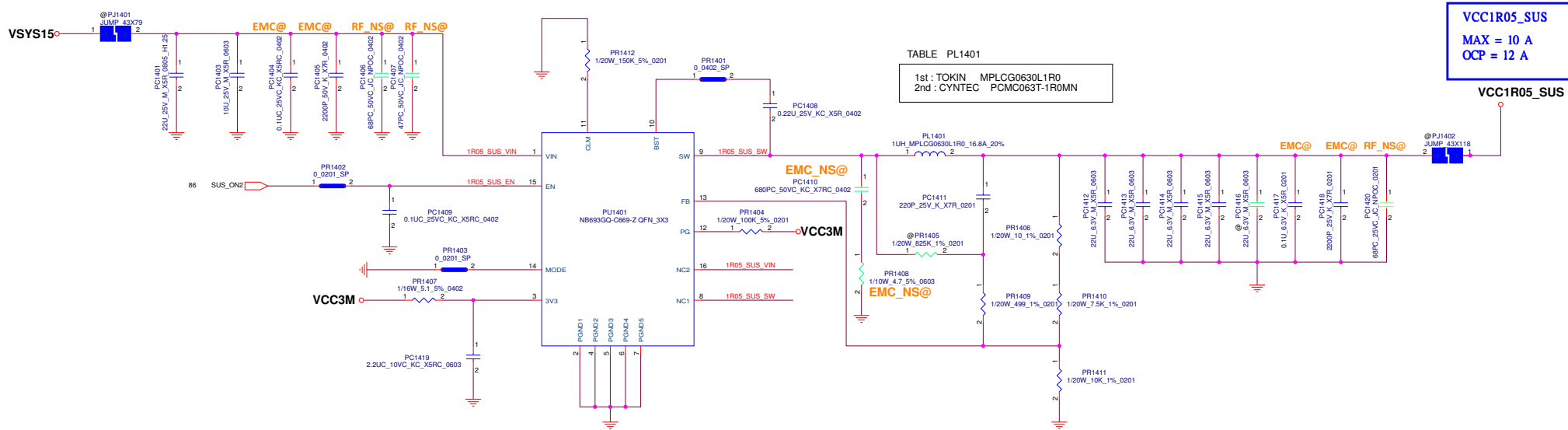
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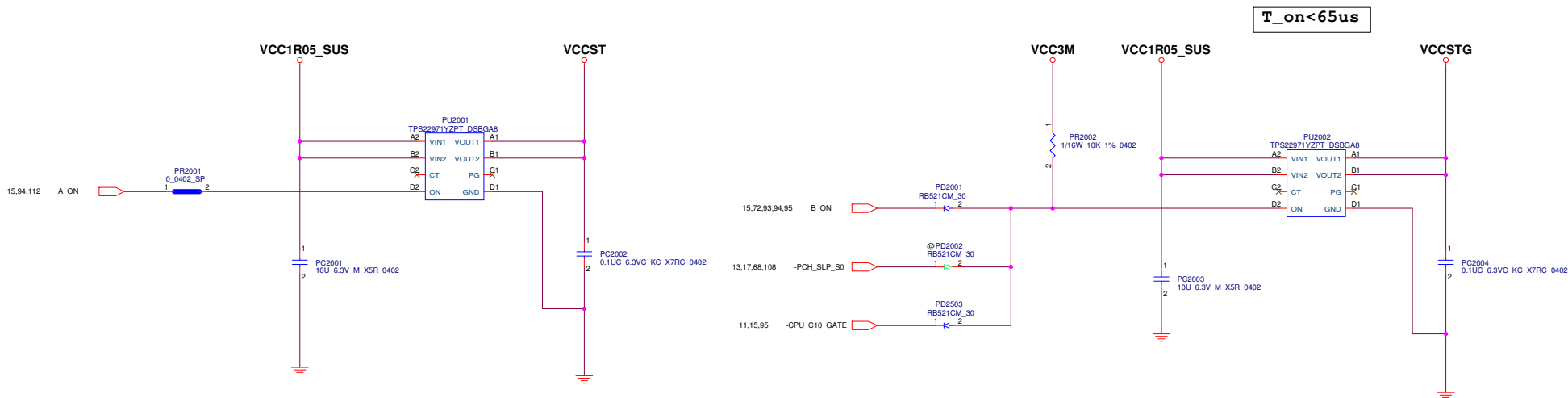
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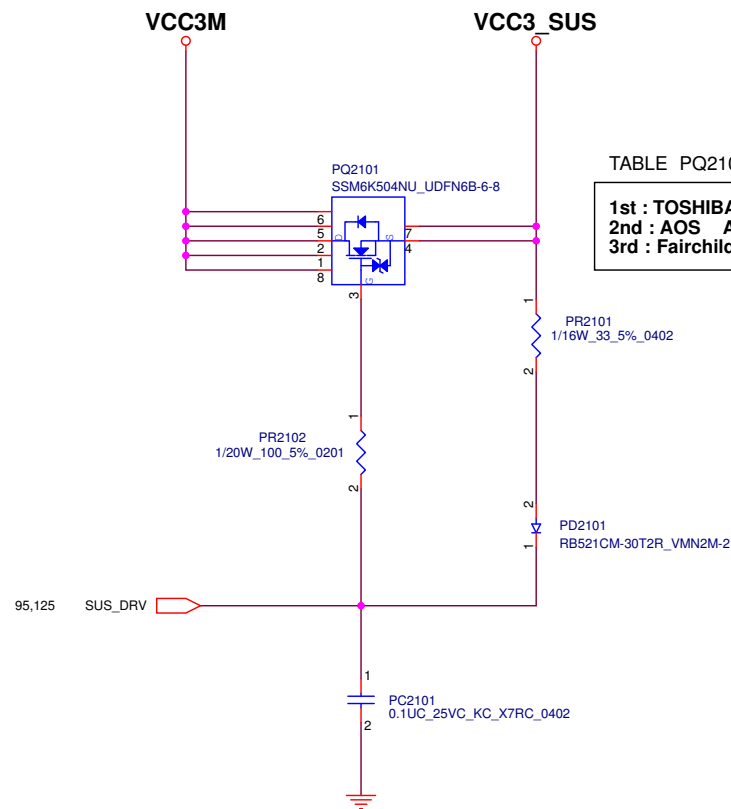




TABLE PQ2101

1st : TOSHIBA SSM6K504NU  
2nd : AOS AON2420  
3rd : Fairchild FDMA8878

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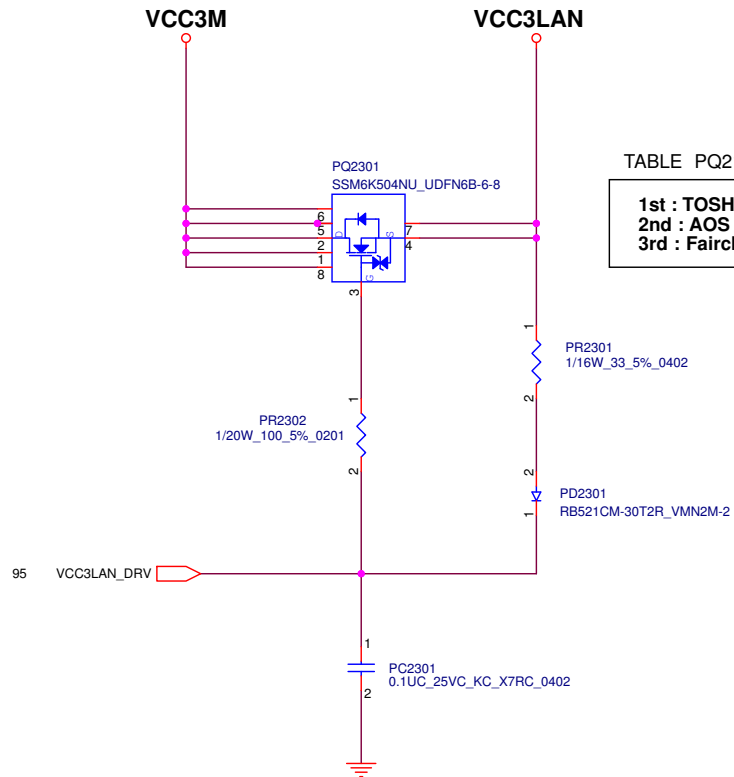



TABLE PQ2101

1st : TOSHIBA SSM6K504NU  
2nd : AOS AON2420  
3rd : Fairchild FDMA8878

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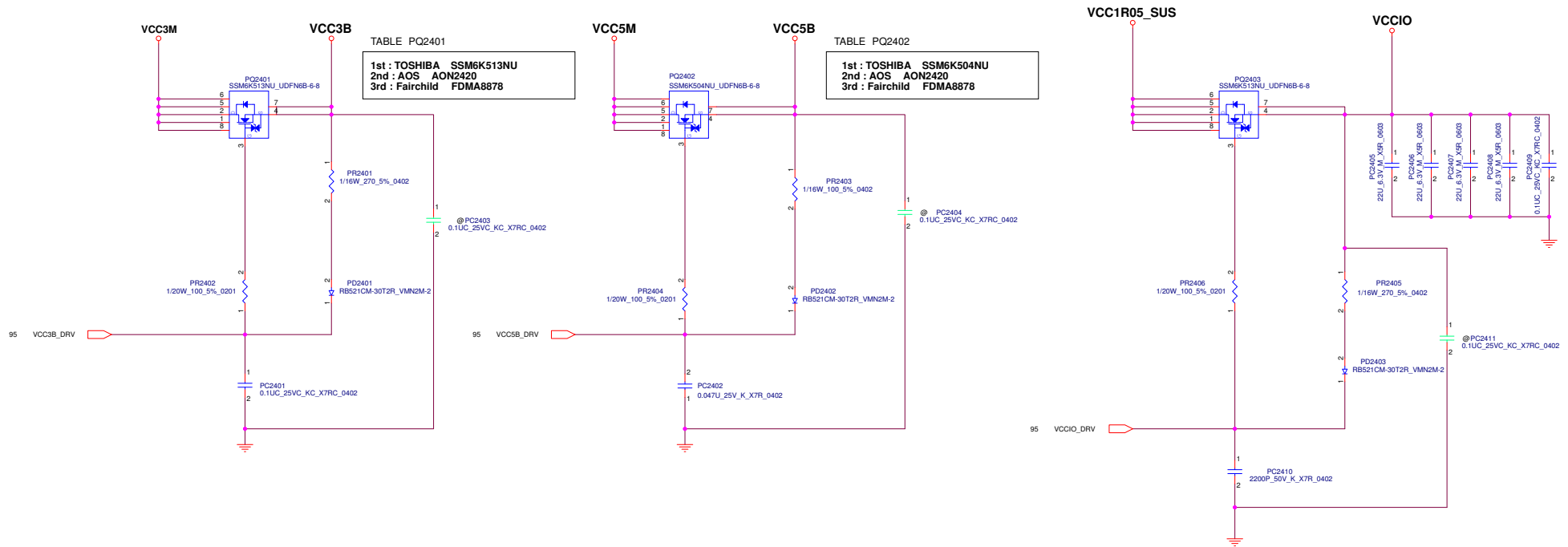


TABLE PQ2401

1st :	TOSHIBA	SSM6K513NU
2nd :	AOS	AON2420
3rd :	Fairchild	FDMA8878

TABLE PQ2402

1st :	TOSHIBA	SSM6K504NU
2nd :	AOS	AON2420
3rd :	Fairchild	FDMA8878

TABLE PQ2403

1st :	TOSHIBA	SSM6K513NU
2nd :	AOS	AON2420
3rd :	Fairchild	FDMA8878

